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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K23

LAST_MODIFIED=Wed Sep 2 16:45:56 2009

REV

ECN

DESCRIPTION OF REVISION

CK APPD / DATE

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0000774489

PRODUCTION RELEASED

2009-08-20

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DRAWING

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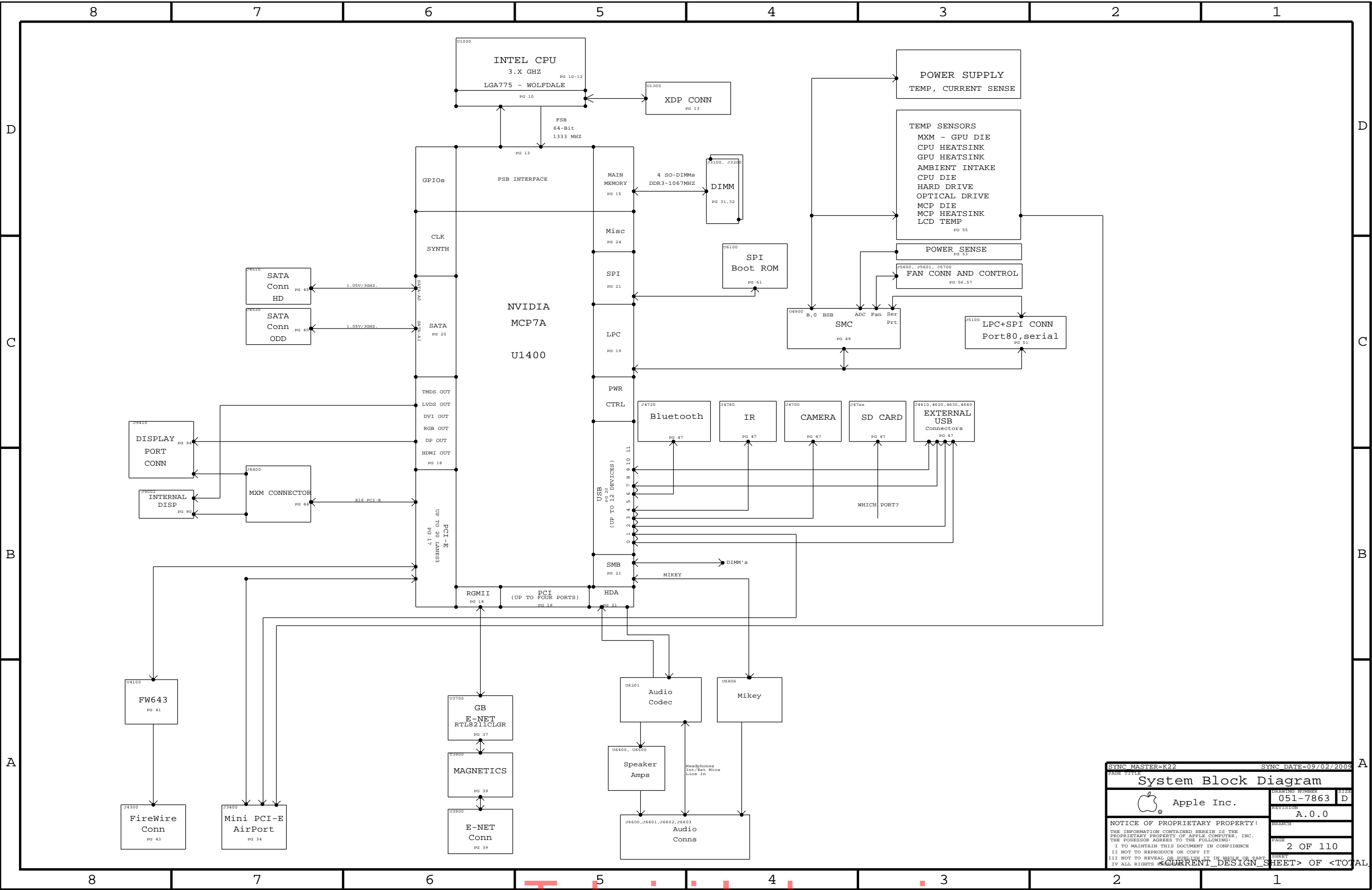
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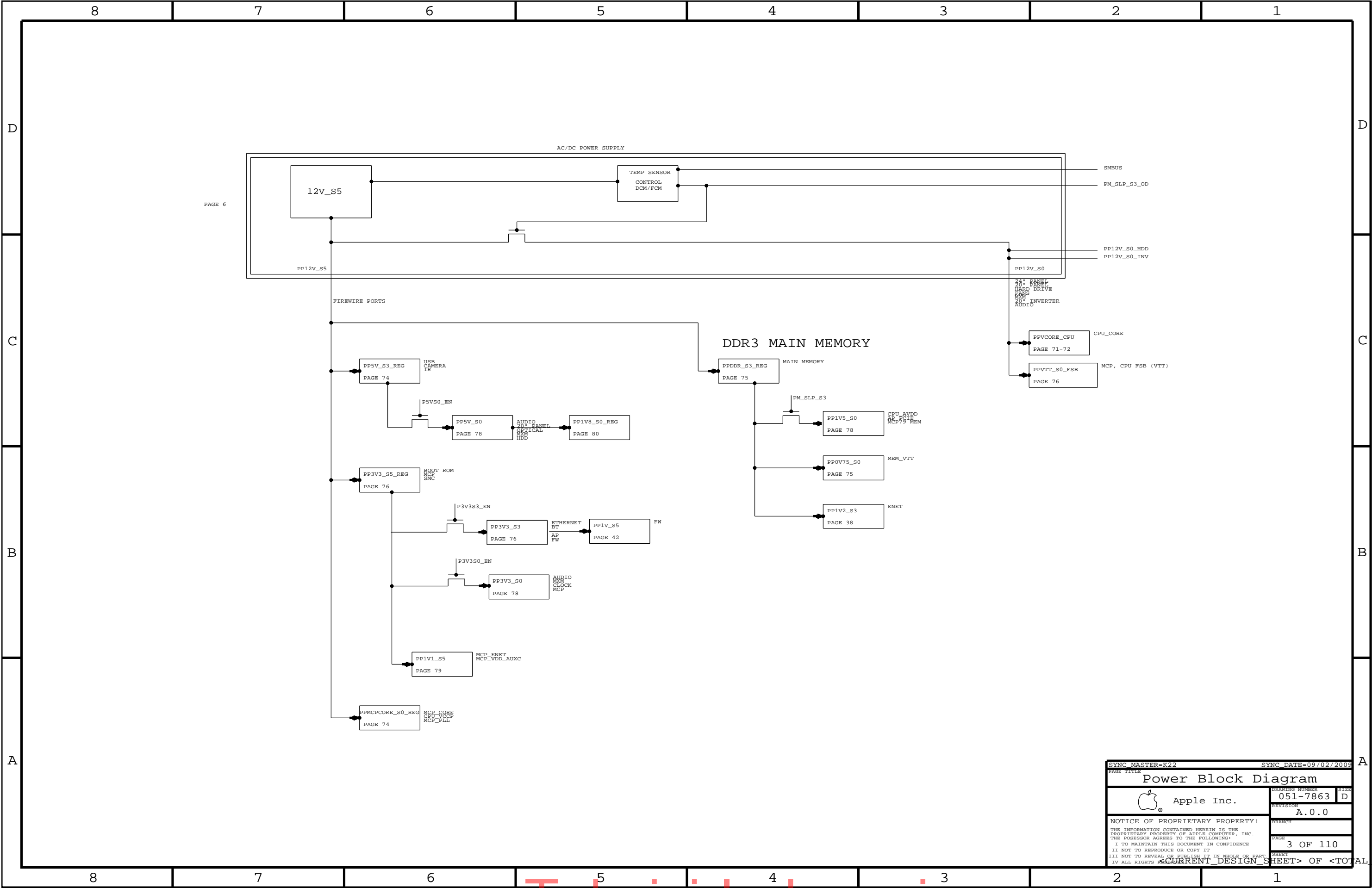
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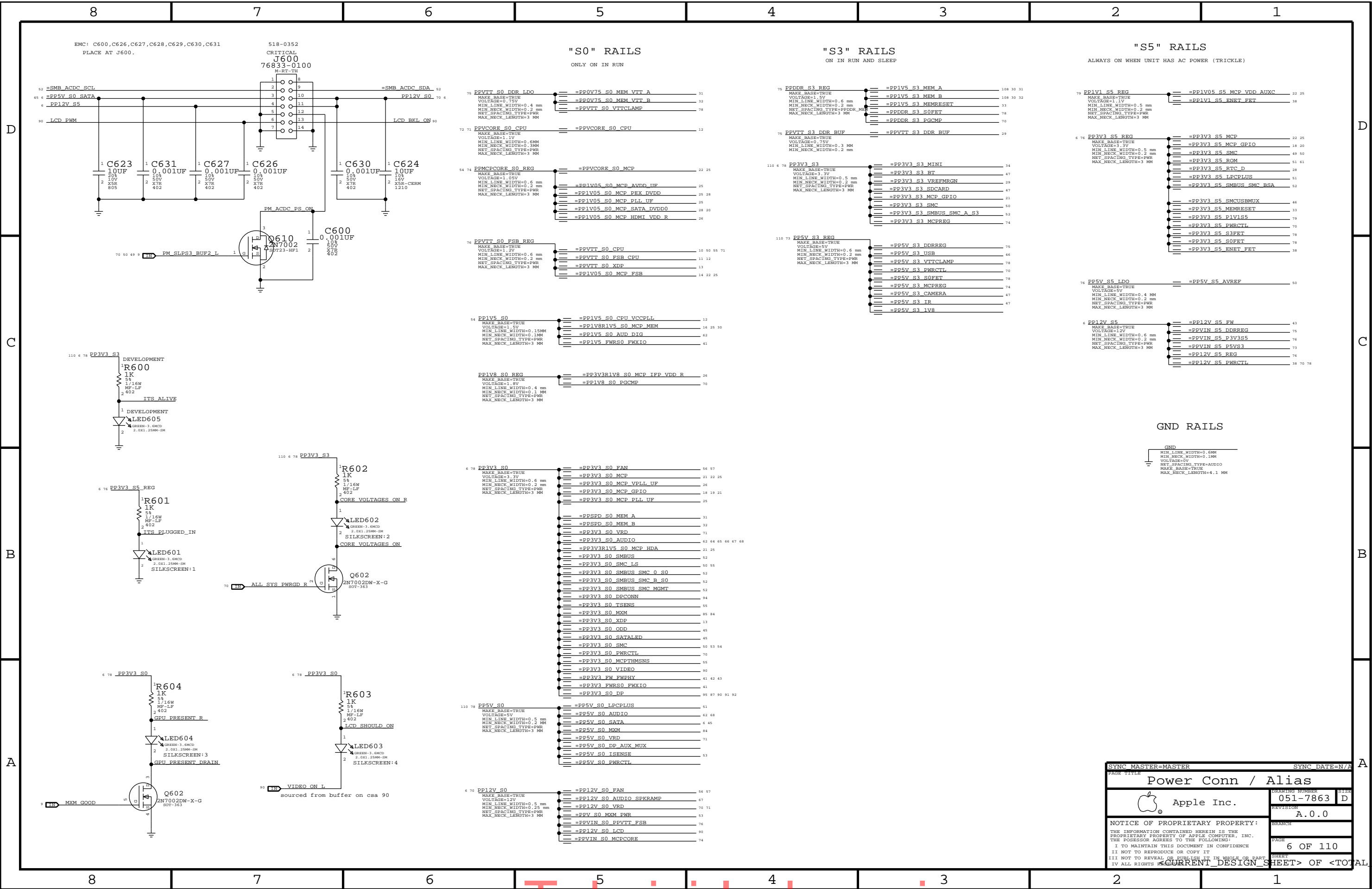
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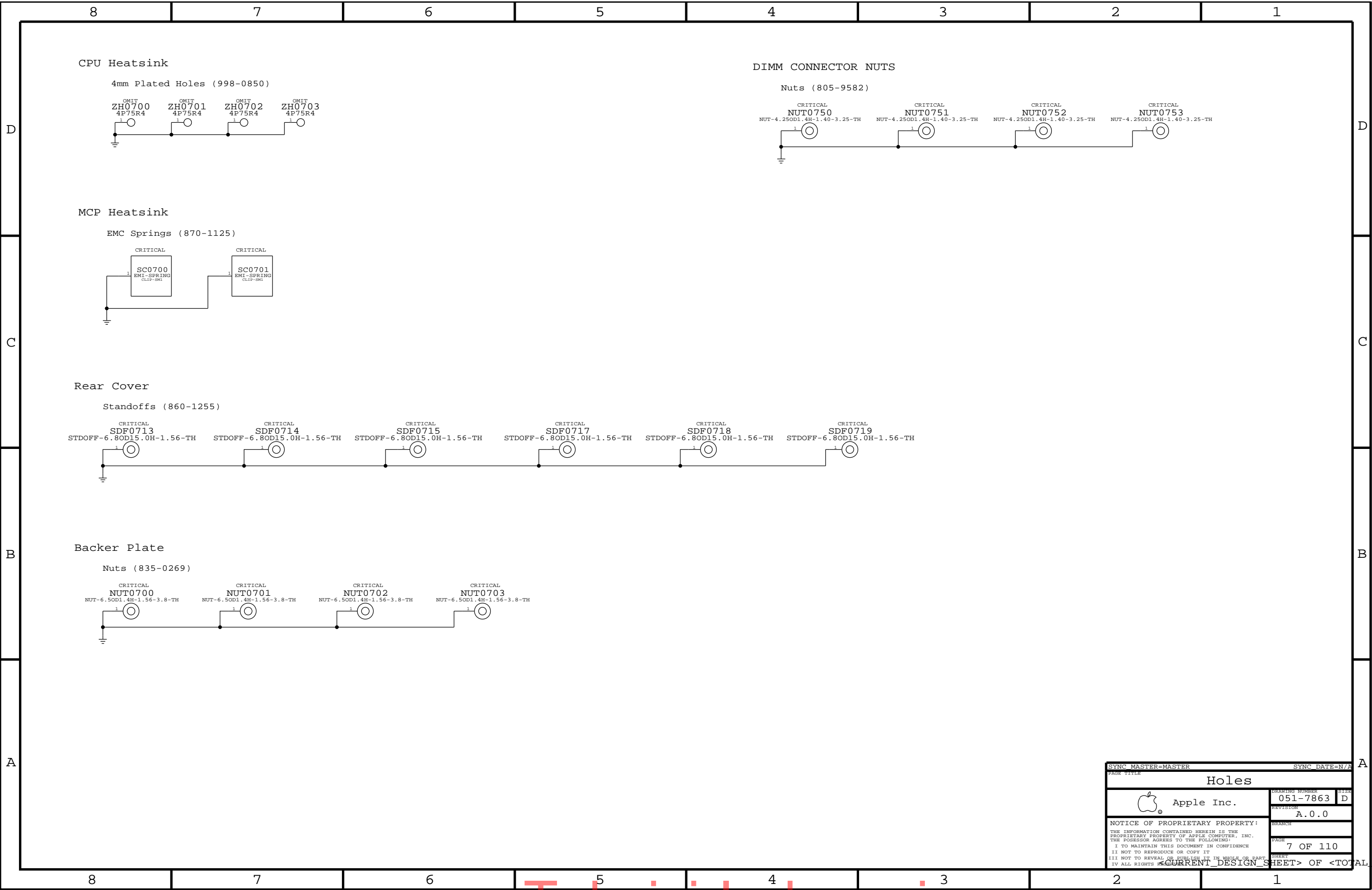



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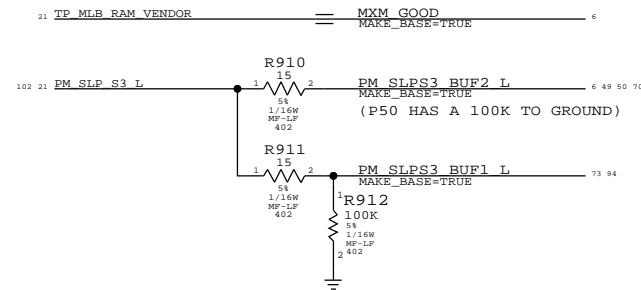
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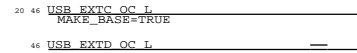
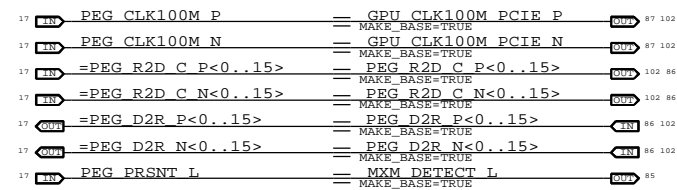


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NC ON UNUSED ALIASES							
18	MCP_TV_DAC_RSET	==	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	MCP_TV_DAC_VREF	==	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	MCP_CLK27M_XTALIN	==	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	MCP_CLK27M_XTALOUT	==	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	CRT_IG_R_C_PR	==	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	CRT_IG_G_Y_Y	==	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	CRT_IG_B_COMP_PB	==	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	CRT_IG_HSYNC	==	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	CRT_IG_VSYNC	==	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	TP_MCP_RGB_HSYNC	==	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	TP_MCP_RGB_VSYNC	==	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_AD<31..15>	==	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_IRDY_L	==	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_C_BE_L<1..0>	==	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_SERR_L	==	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_DEVSEL_L	==	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_PERR_L	==	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_LPC_DRQ0_L	==	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
21	TP_MCP_BUF_SIO_CLK	==	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	TP_ENET_INTR_L	==	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
18	TP_ENET_PWRDWN_L	==	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
21	TP_MCP_KBDRSTIN_L	==	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
	TP_MCP_GPIO_18	==	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE		
21	TP_MLB_RAM_SIZE	==	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_C_BE_L<3>	==	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_CLK0	==	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_CLK1	==	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_FRAME_L	==	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_GNT0_L	==	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_GNT1_L	==	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_INTW_L	==	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_INTX_L	==	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_INTY_L	==	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_INTZ_L	==	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_PAR	==	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_RESET1_L	==	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_STOP_L	==	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_TRDY_L	==	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE4N	==	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE4P	==	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE5N	==	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE5P	==	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE6P	==	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_CLK100M_PE6N	==	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_EXCARD_PRSNT_L	==	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PE4_CLKREQ_L	==	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PE4_PRSNT_L	==	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
21	TP_SB_A20GATE	==	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	TP_USB_10N	==	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	TP_USB_10P	==	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_MINI_N	==	NC_USB_MINI_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_MINI_P	==	NC_USB_MINI_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_EXCARD_N	==	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_EXCARD_P	==	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
21	ODD_PWR_EN_L	==	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_CLK100M_EXCARD_P	==	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_CLK100M_EXCARD_N	==	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	EXCARD_CLKREQ_L	==	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_AD<12..10>	==	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	TP_PCI_AD<8>	==	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_PE4_R2D_CP	==	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_PE4_R2D_CN	==	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_PE4_D2RP	==	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	TP_PCIE_PE4_D2RN	==	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_EXCARD_D2R_P	==	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_EXCARD_D2R_N	==	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_EXCARD_R2D_C_P	==	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	PCIE_EXCARD_R2D_C_N	==	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_TPAD_N	==	NC_USB_TPAD_N	MAKE_BASE=TRUE	NO_TEST=TRUE		
20	USB_TPAD_P	==	NC_USB_TPAD_P	MAKE_BASE=TRUE	NO_TEST=TRUE		
MCP HAS INTERNAL 15K PULL-DOWNS							
UNUSED MEMORY SIGNALS							
15	TP_MEM_A_CLK2P	==	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE		
15	TP_MEM_A_CLK2N	==	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE		
16	TP_MEM_A_CLK5P	==	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE		
16	TP_MEM_A_CLK5N	==	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE		
15	TP_MEM_B_CLK2P	==	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE		
15	TP_MEM_B_CLK2N	==	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE		
16	TP_MEM_B_CLK5P	==	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE		
16	TP_MEM_B_CLK5N	==	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE		
UNUSED GMUX JTAG FROM MCP							
17	GMUX_JTAG_TCK_L	==	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE		
17	GMUX_JTAG_TDO	==	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	GMUX_JTAG_TDI	==	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE		
19	GMUX_JTAG_TMS	==	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE		
SYNC MASTER=K22 SYNC DATE=09/02/2009							
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UNUSED SIGNAL ALIAS							
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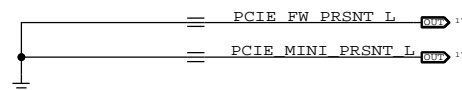
SIGNAL ALIAS



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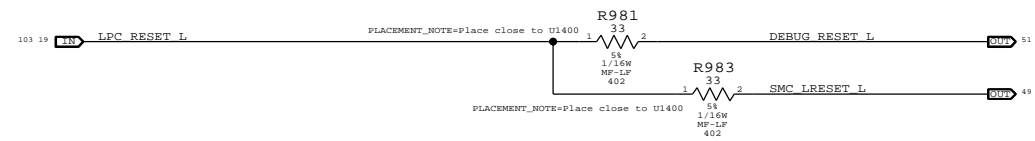


K22/K23 Use one GPIO for both ports 2&3 OC
USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

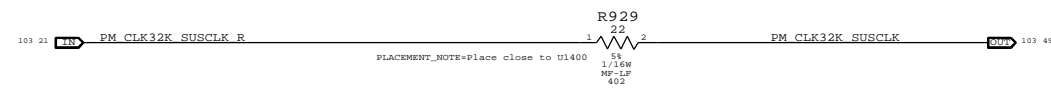
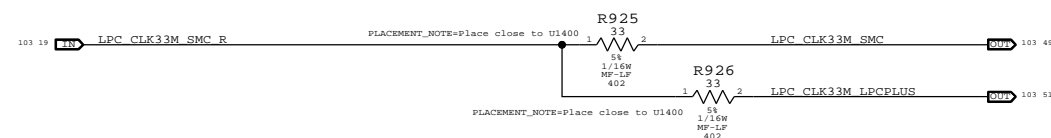
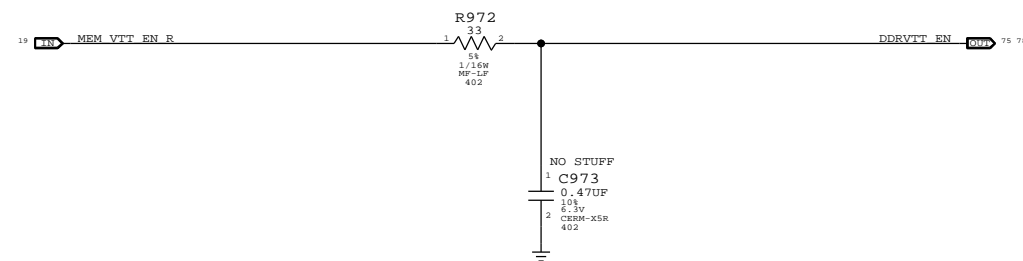
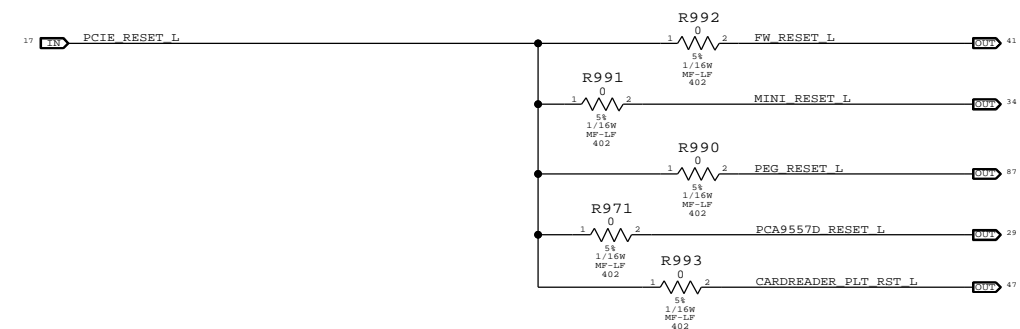


Platform Reset Connections

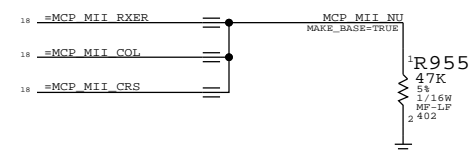
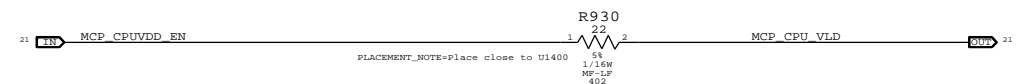
LPC Reset (Unbuffered)




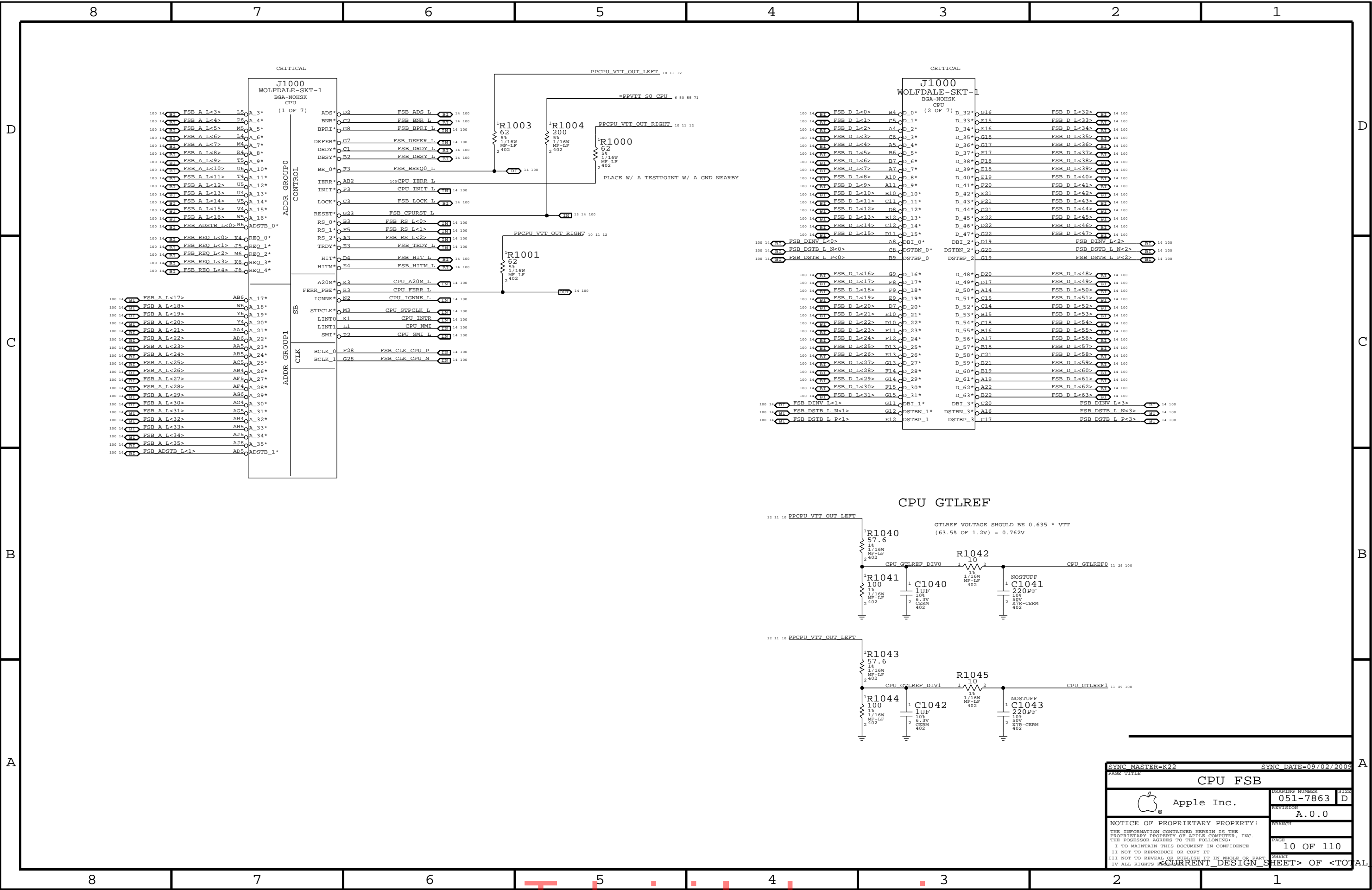
PCIE Reset (Unbuffered)

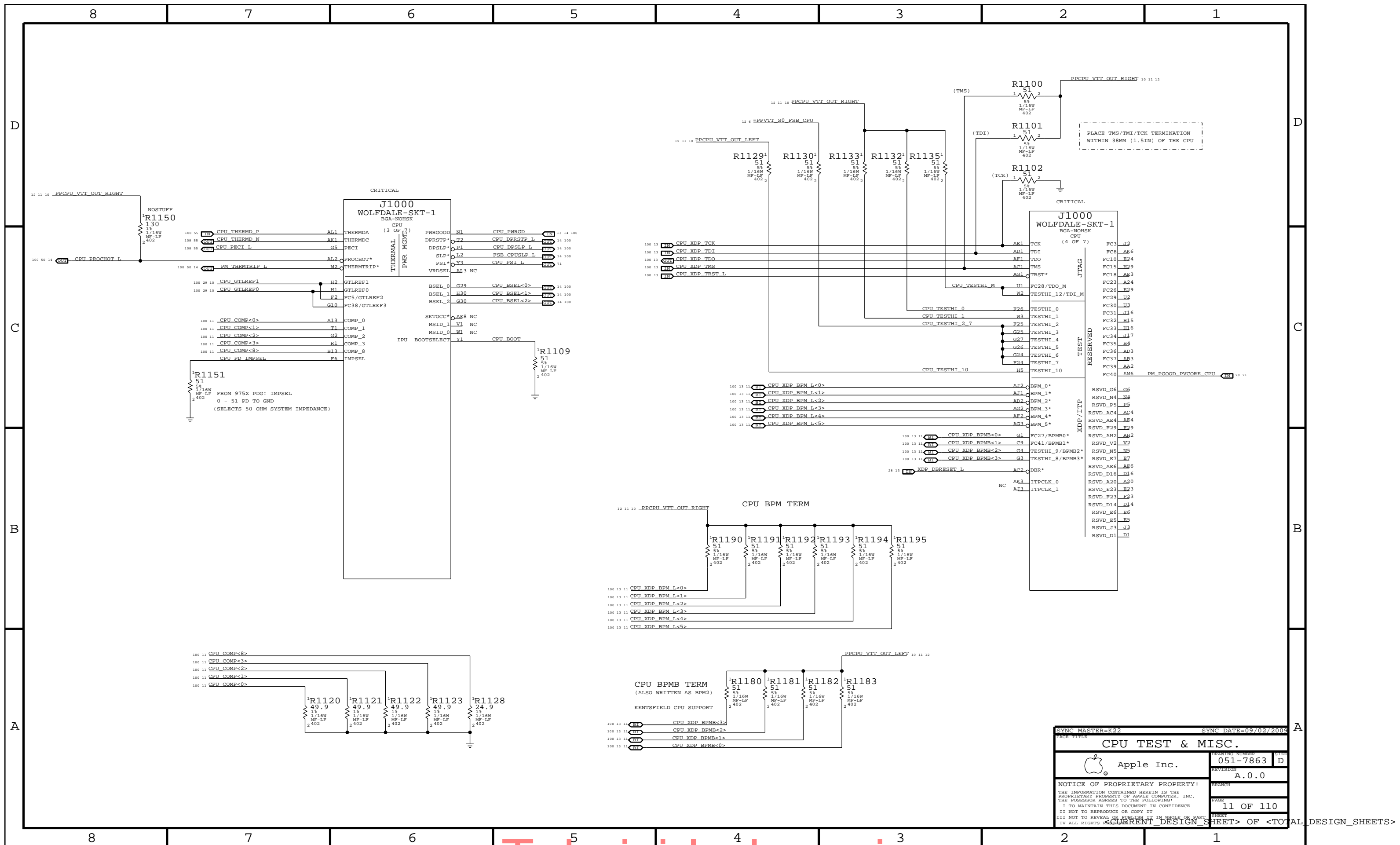


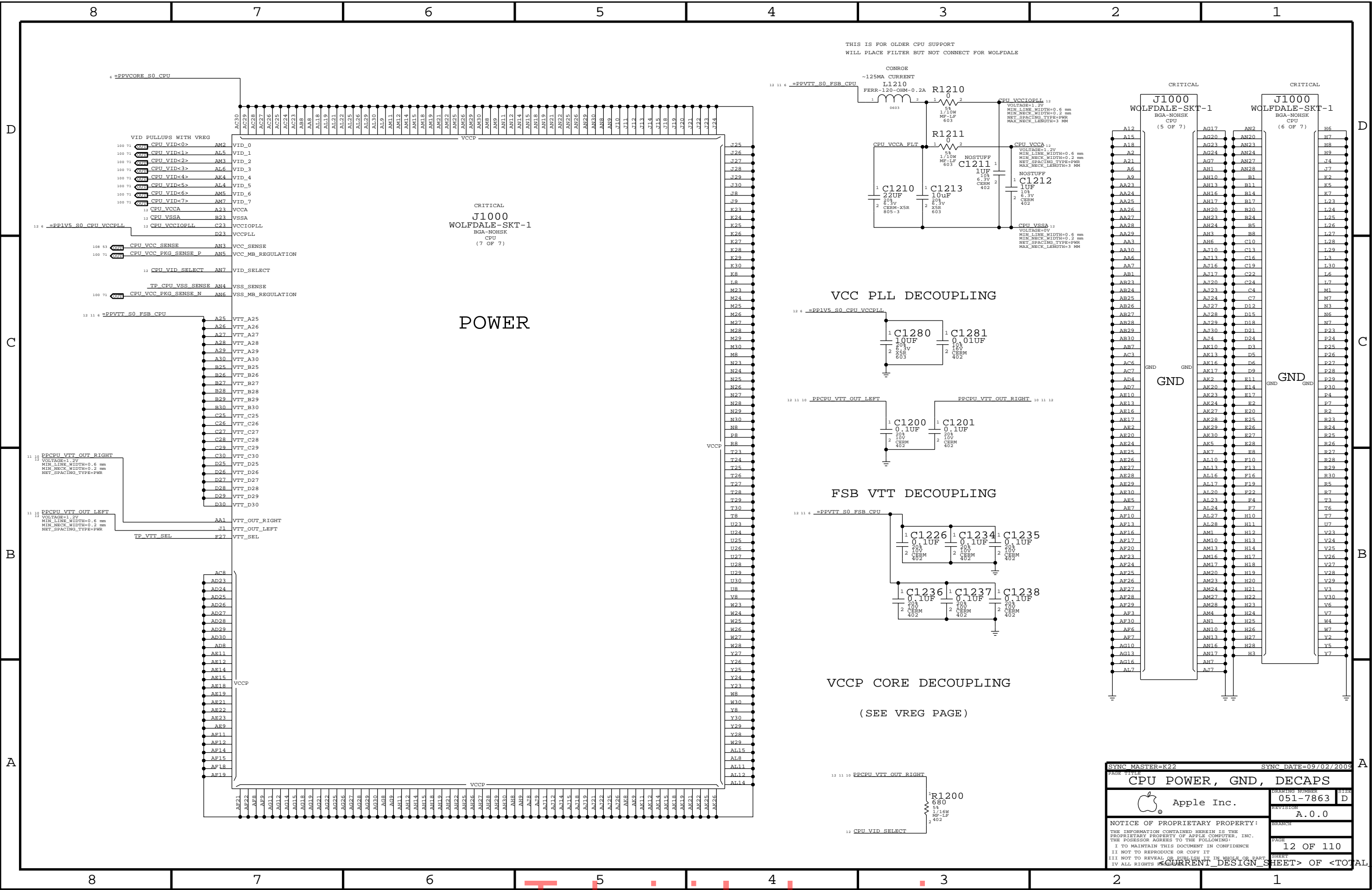
MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

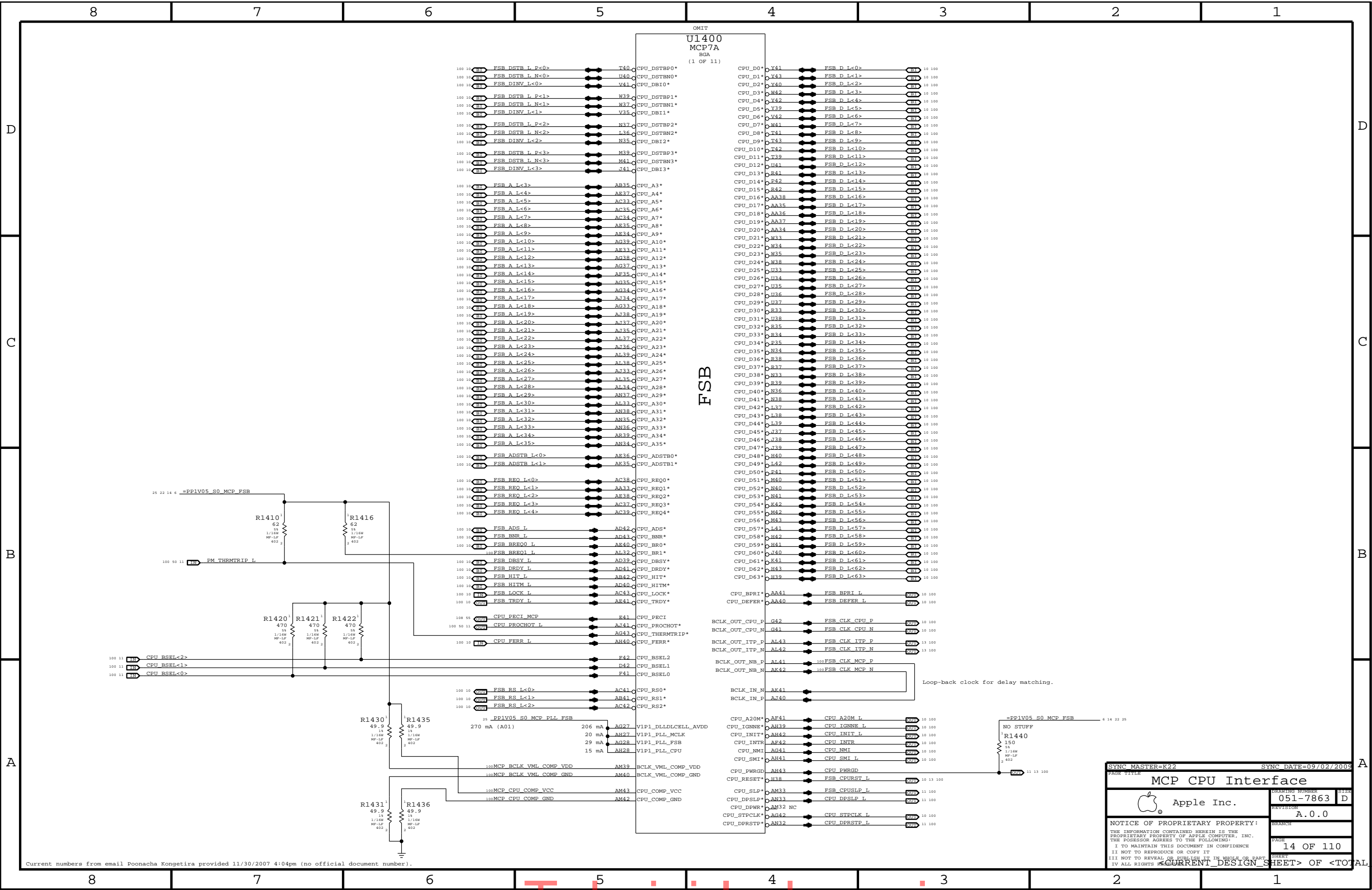


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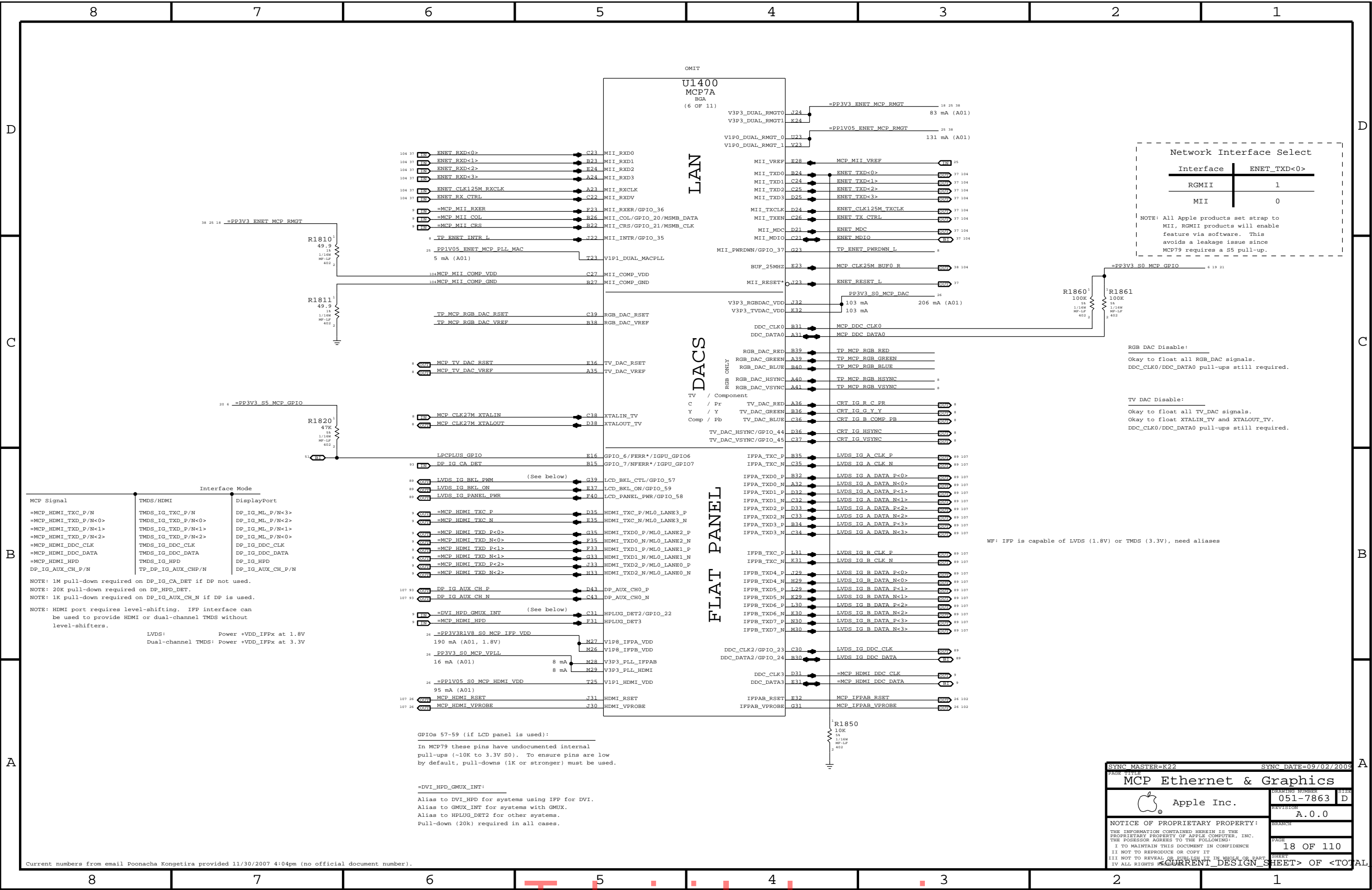


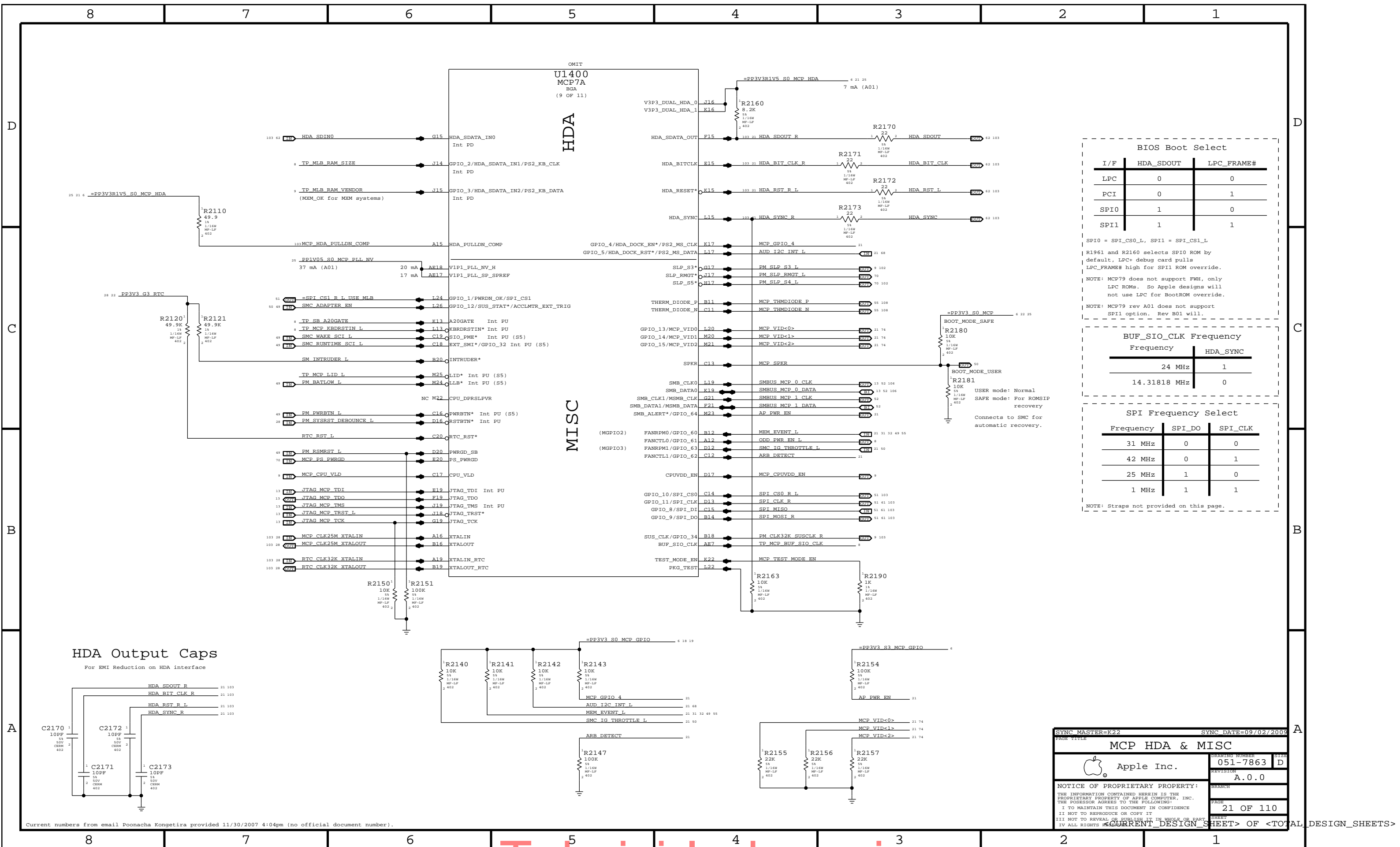


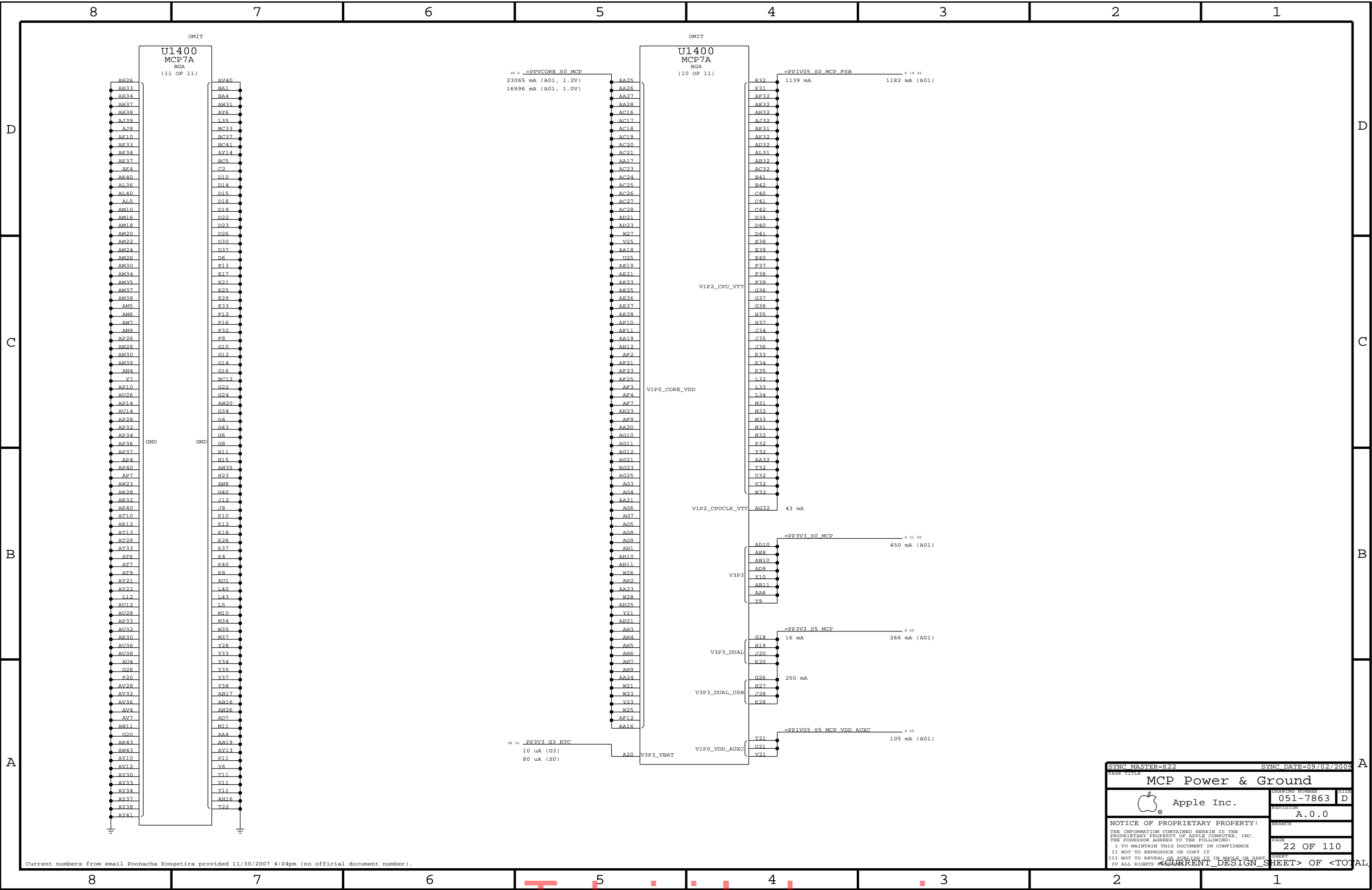














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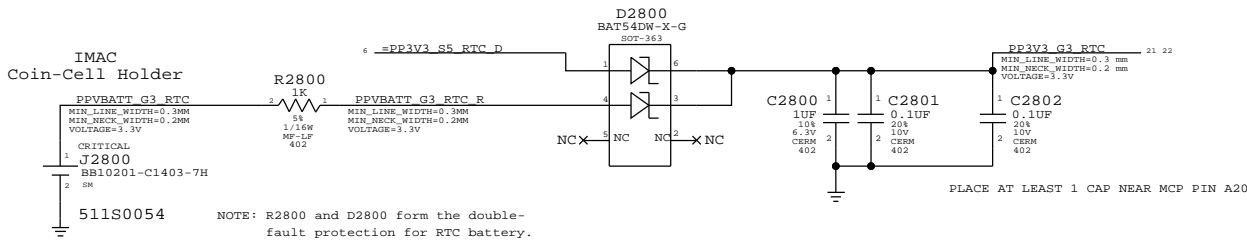
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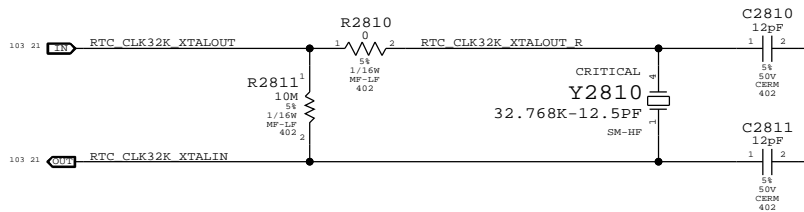
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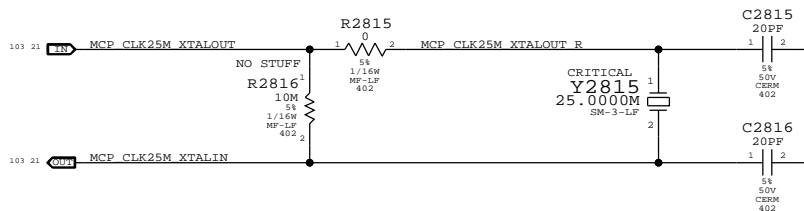
RTC Power Sources



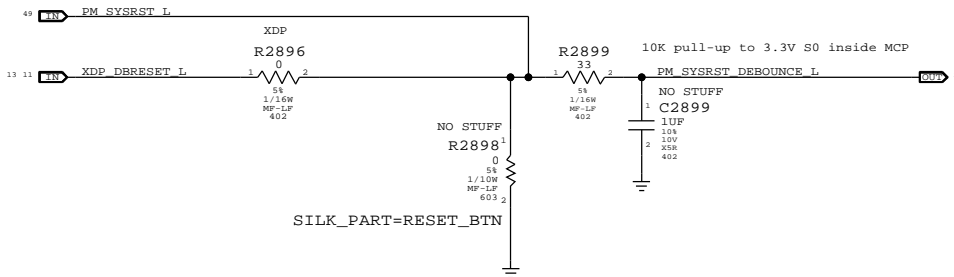
RTC Crystal



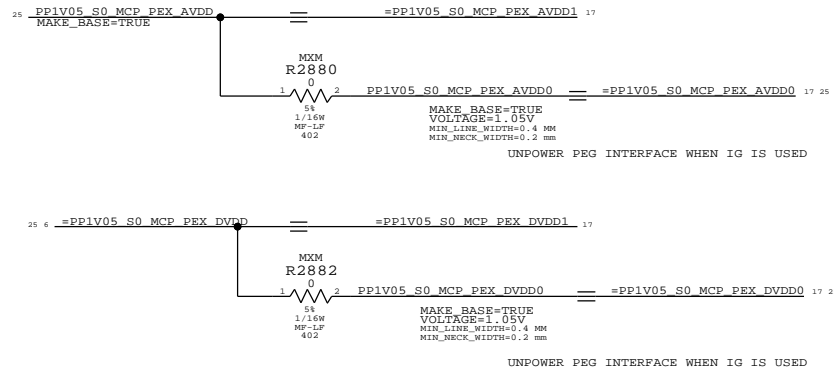
MCP 25MHz Crystal



Reset Button

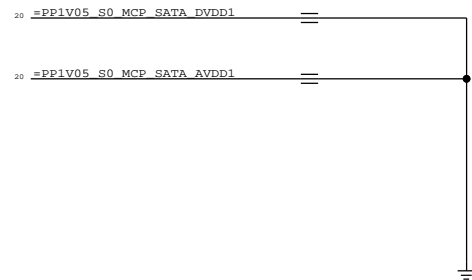
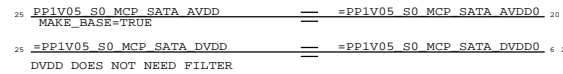


PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1

AVDD IS FILTERED ON P2



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

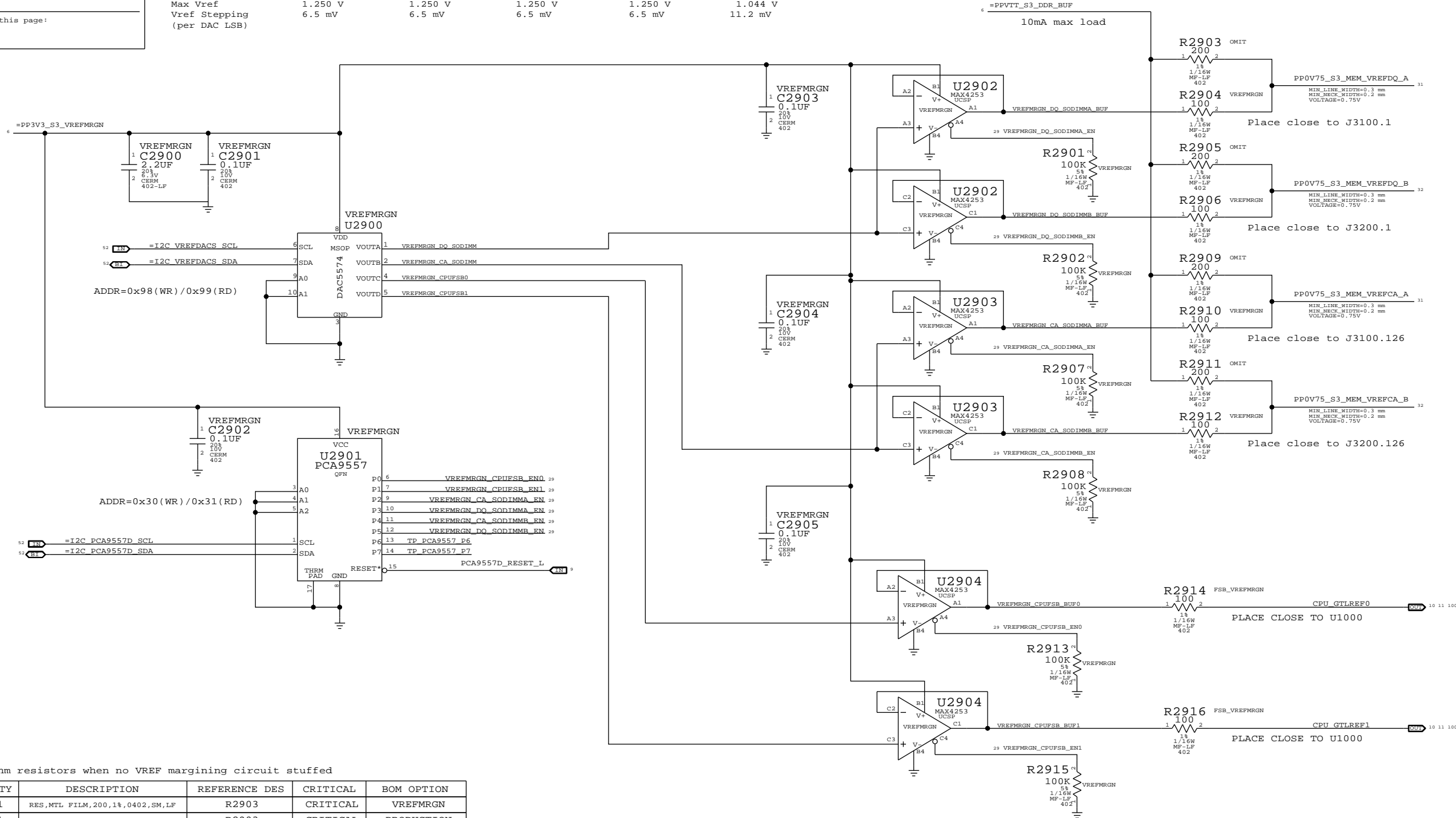
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
A	0x00	0x00	0x00	0x00	0x00
B	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

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FSB/DDR3 Vref Margining

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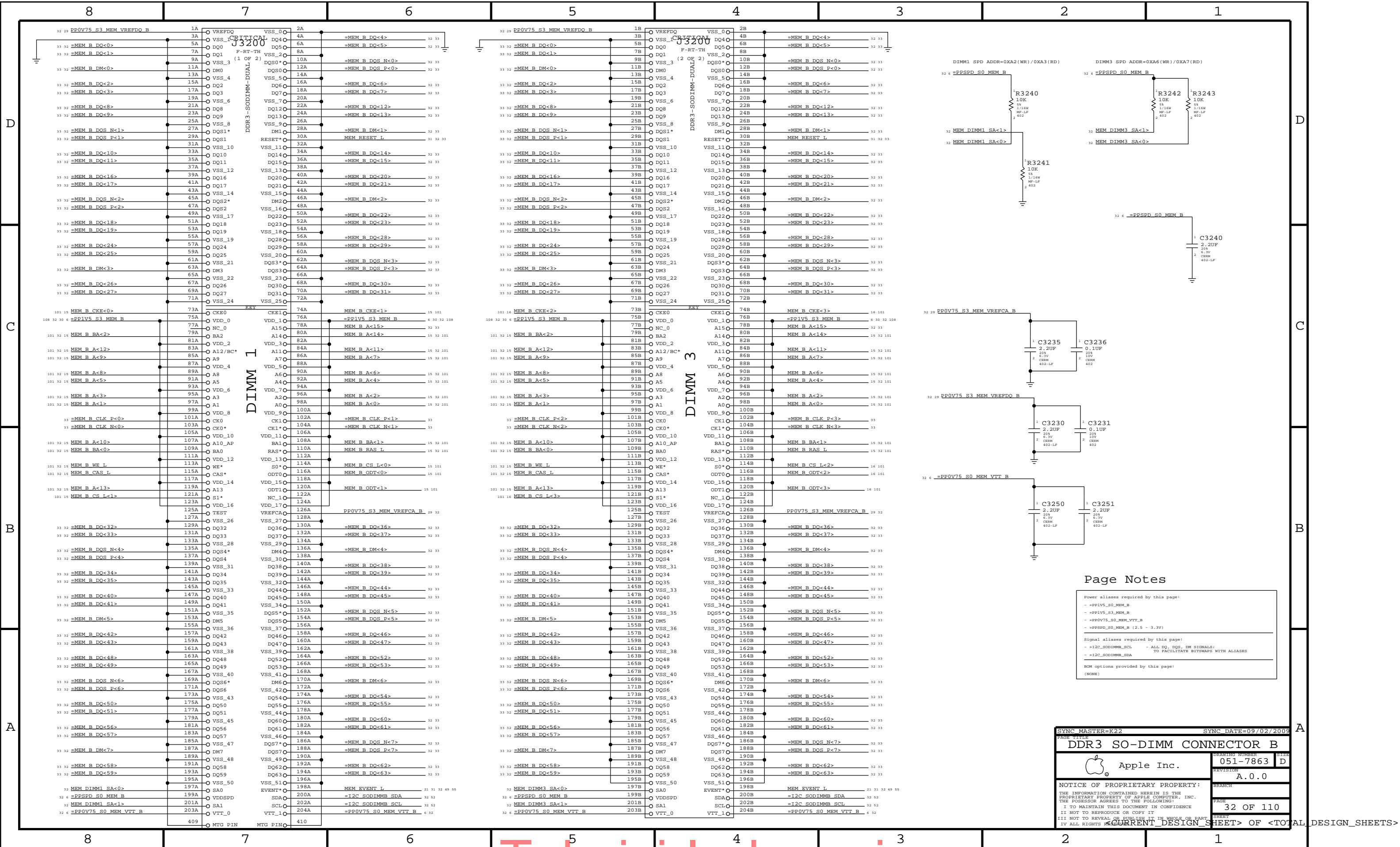
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DDR3 SO-DIMM CONNECTOR B

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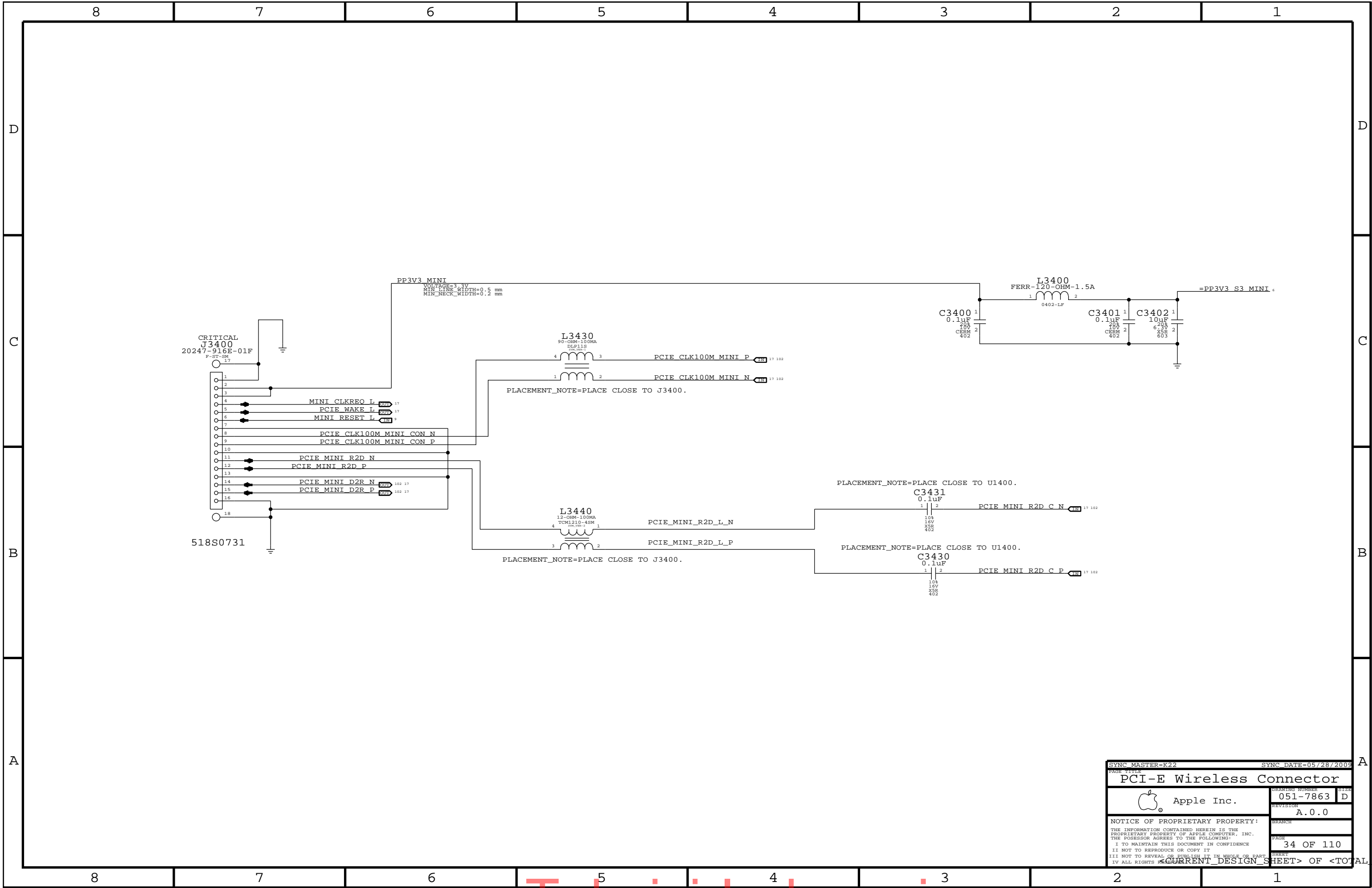
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PCI-E Wireless Connector			
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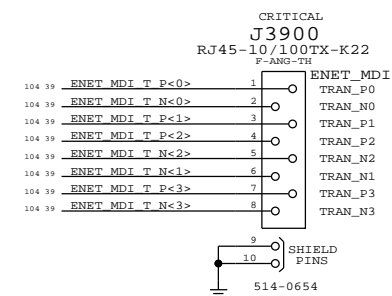
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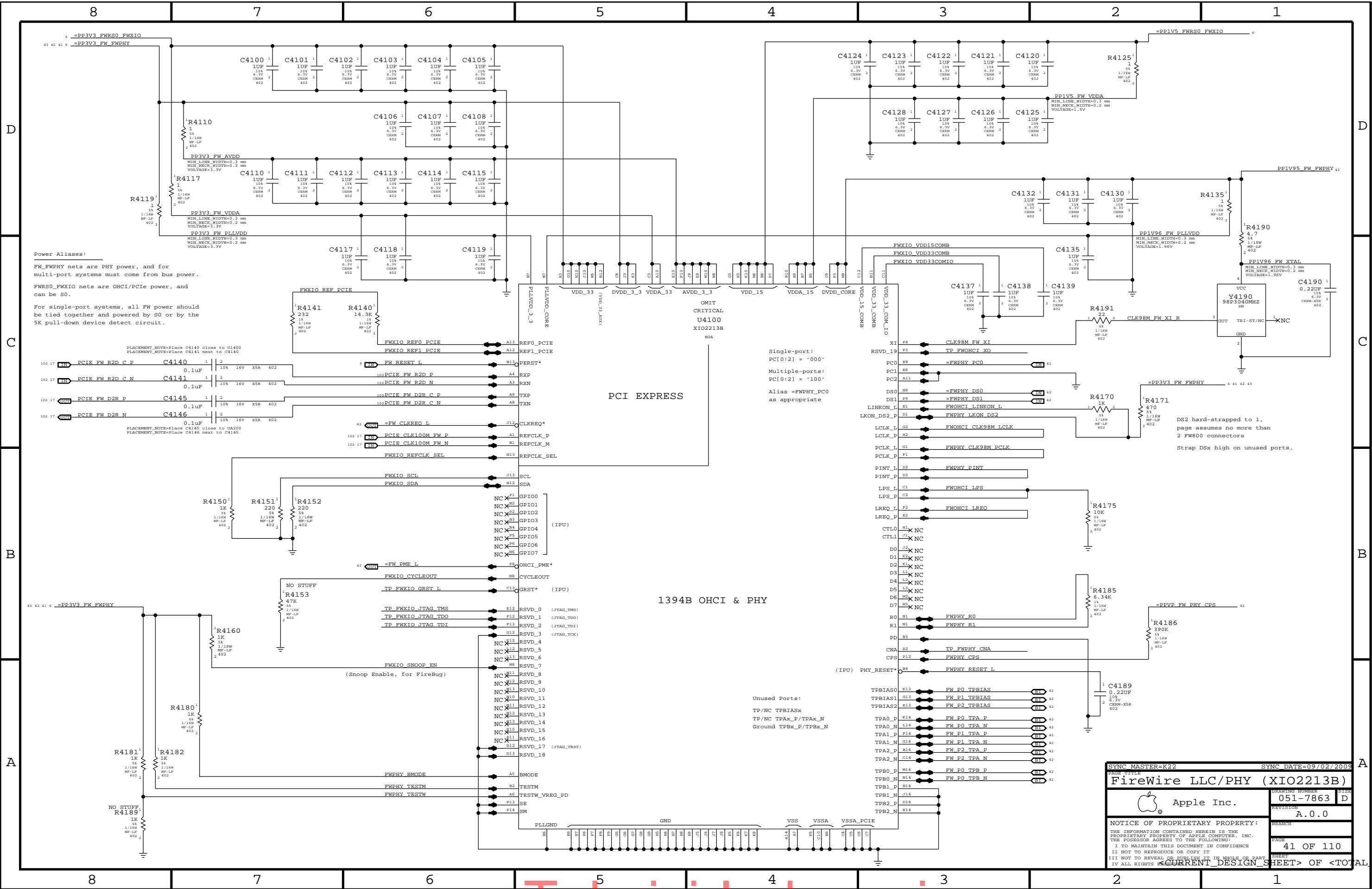
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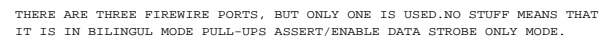
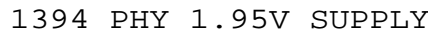
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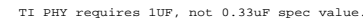
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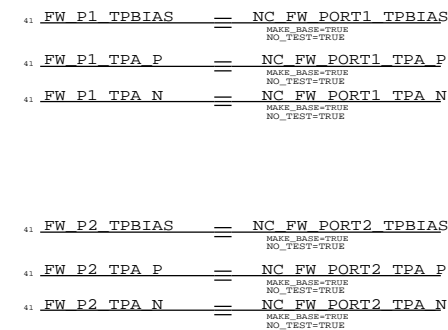
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iMacs are now one port only and have Power Code "000"



TI PHY "Peaking Inductors" To improve Data Eye




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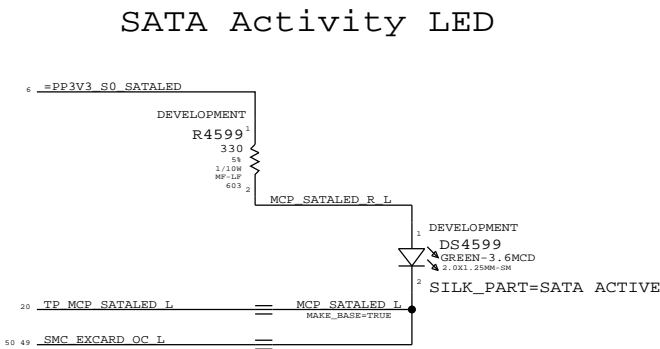
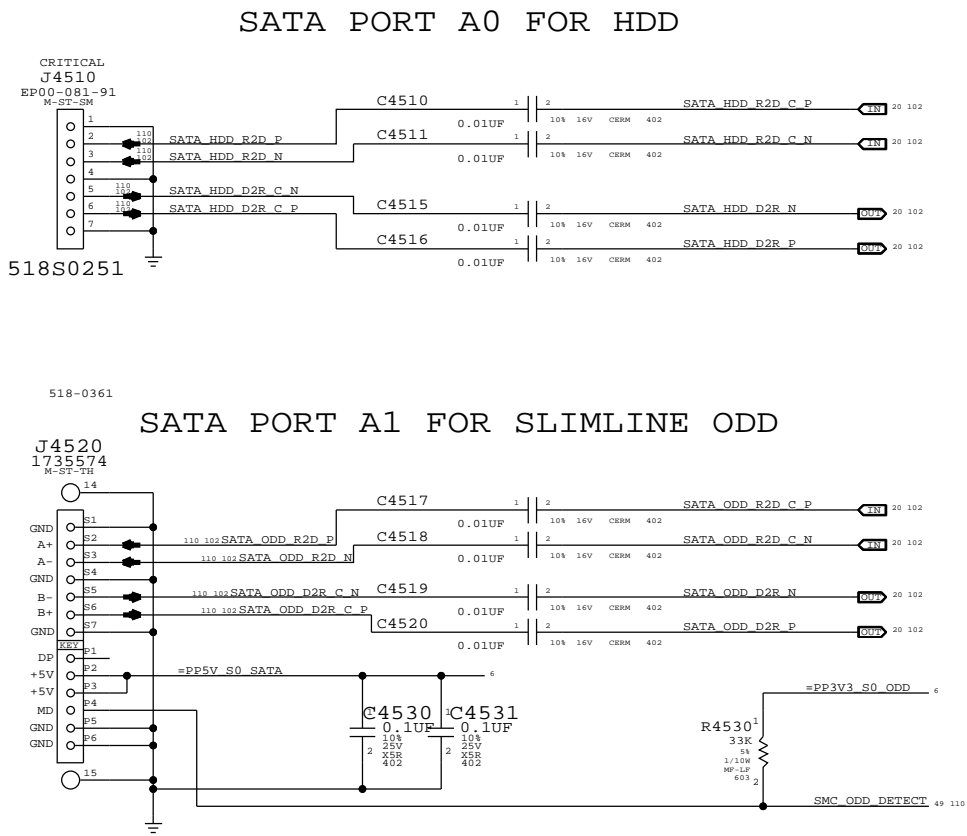
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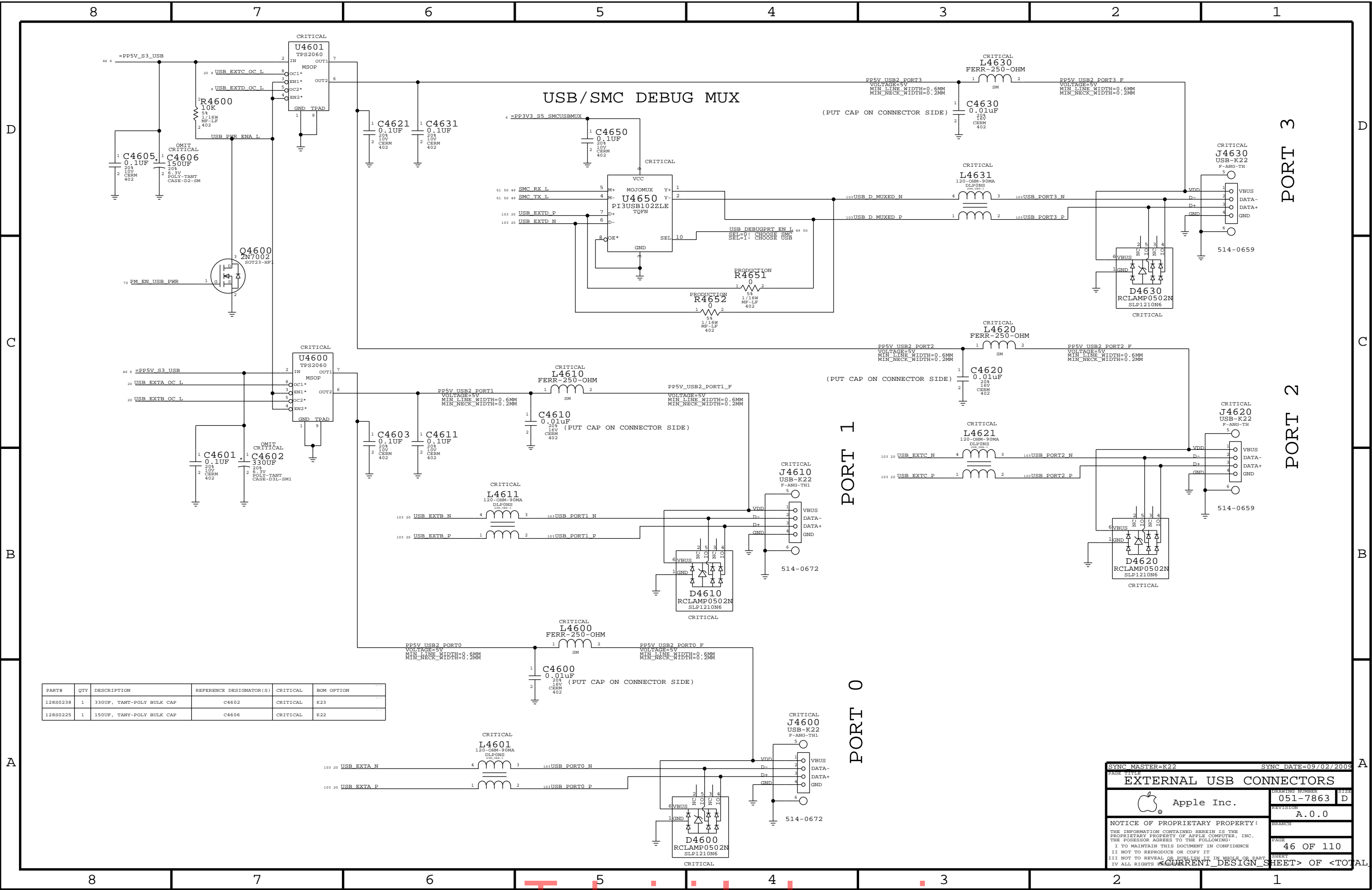
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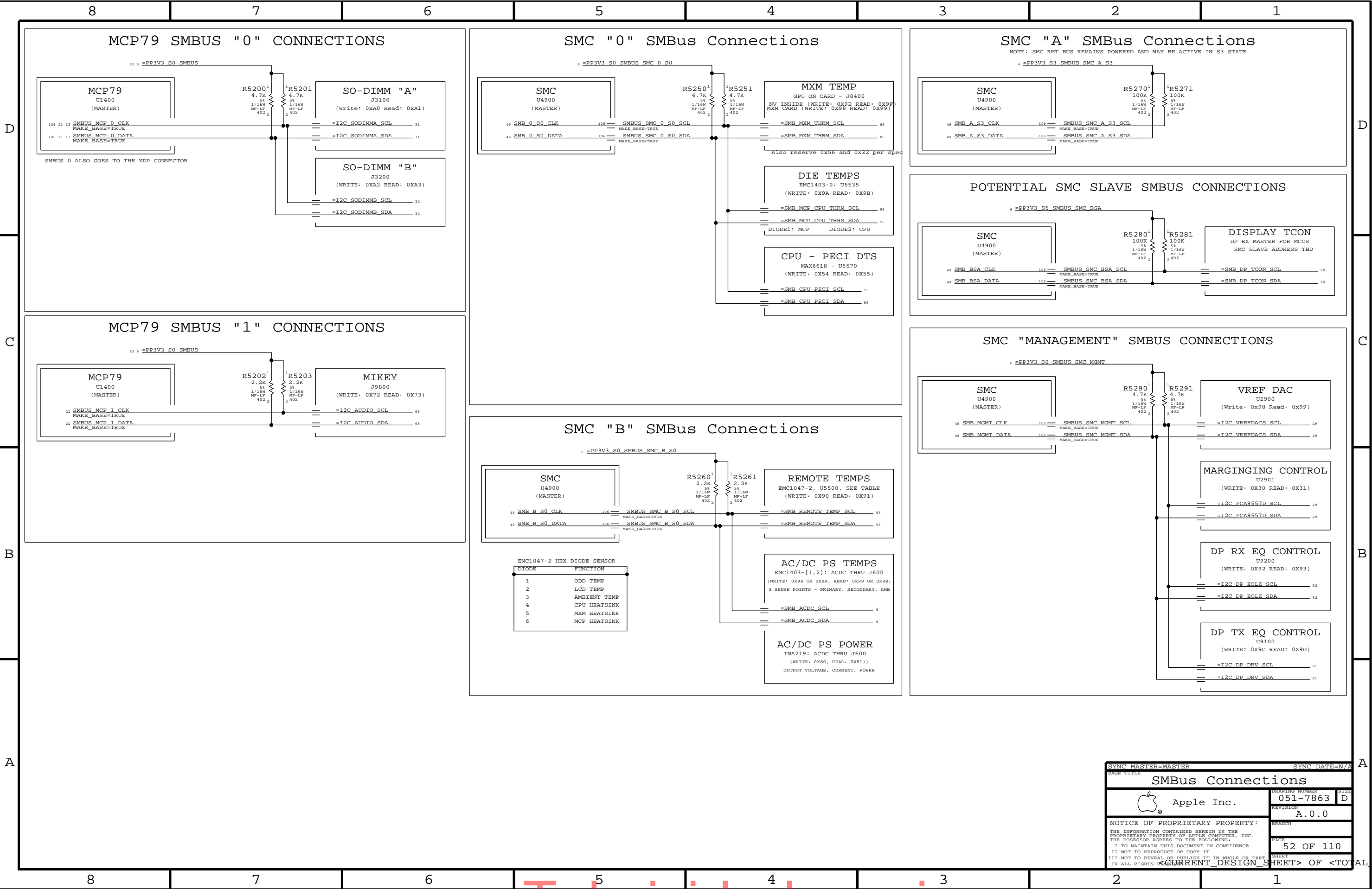


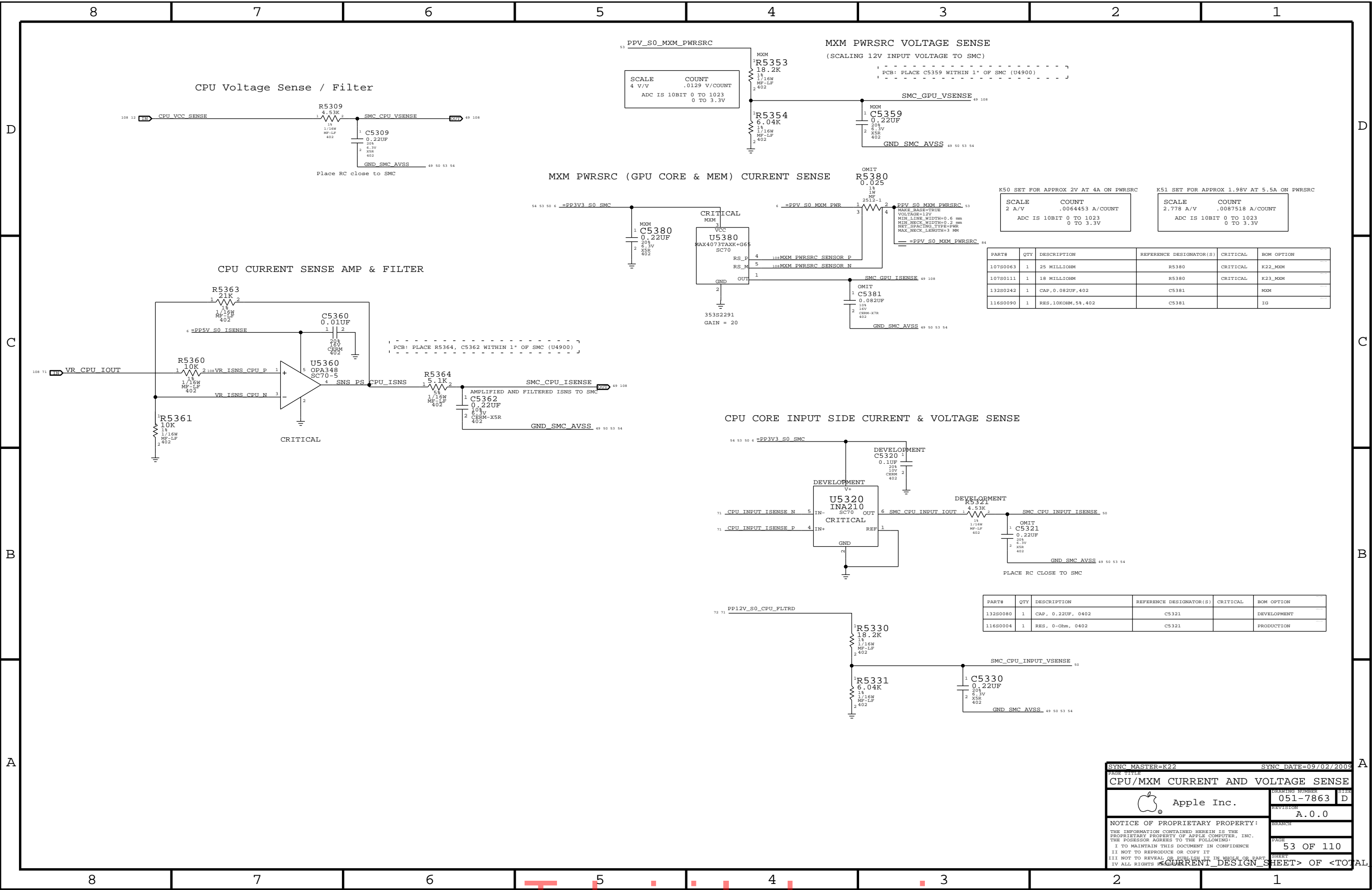
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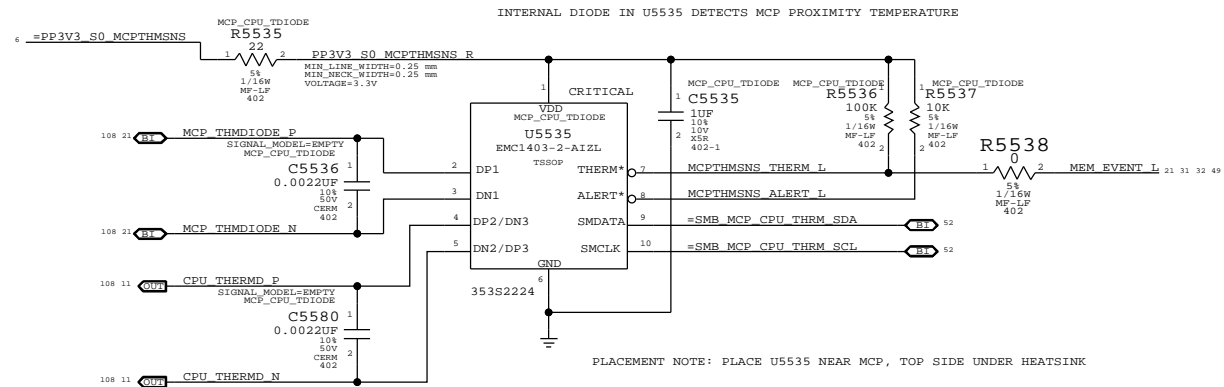
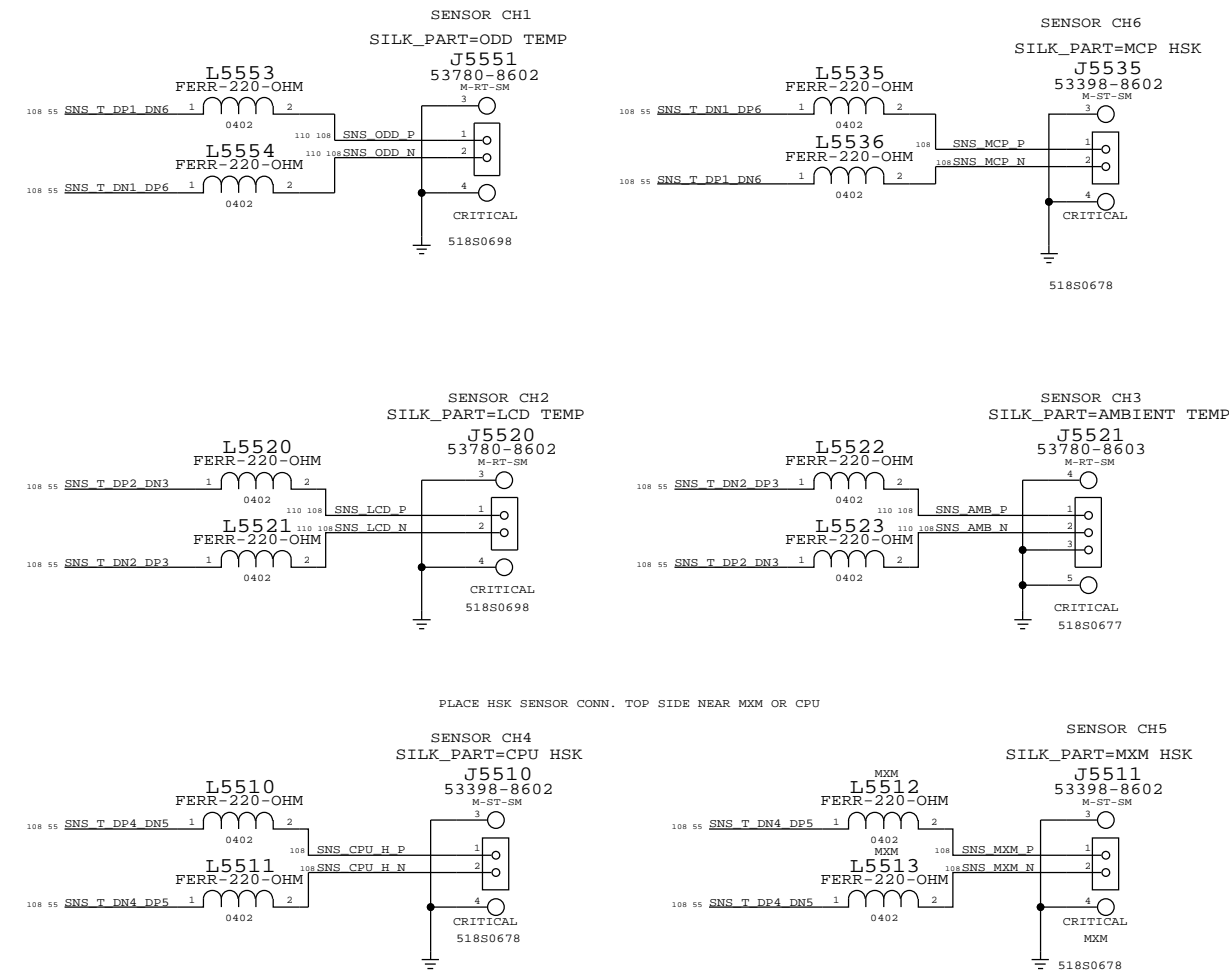
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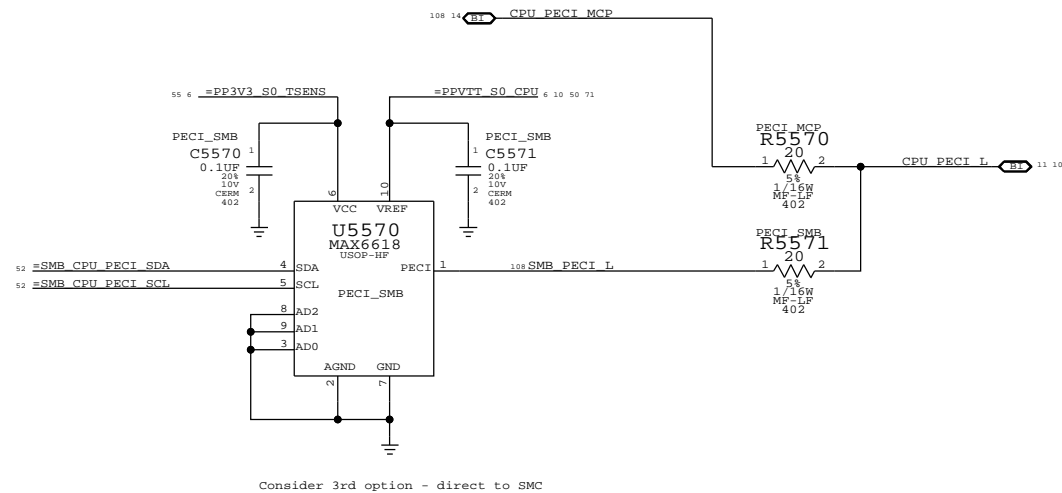


REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

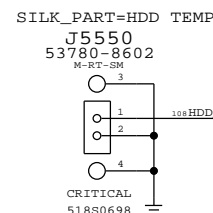
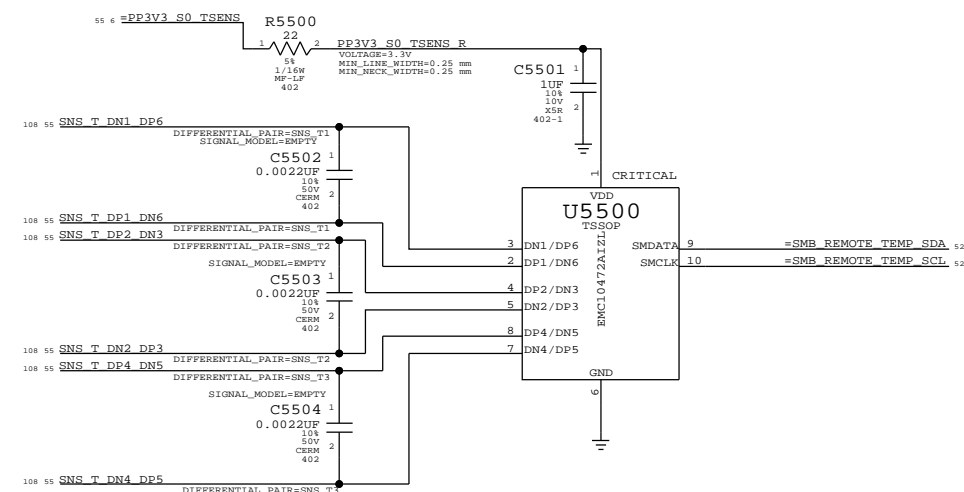
MCP & CPU T-Diode Thermal Sensor



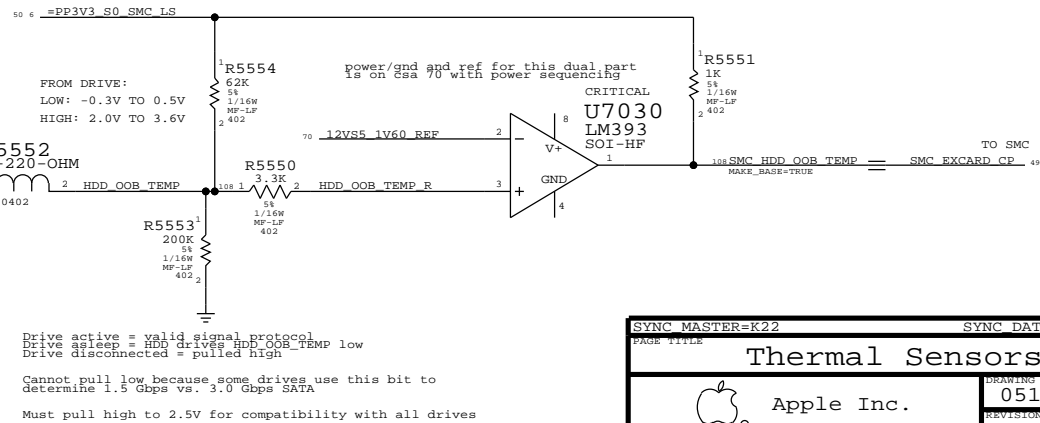
CPU PECCI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



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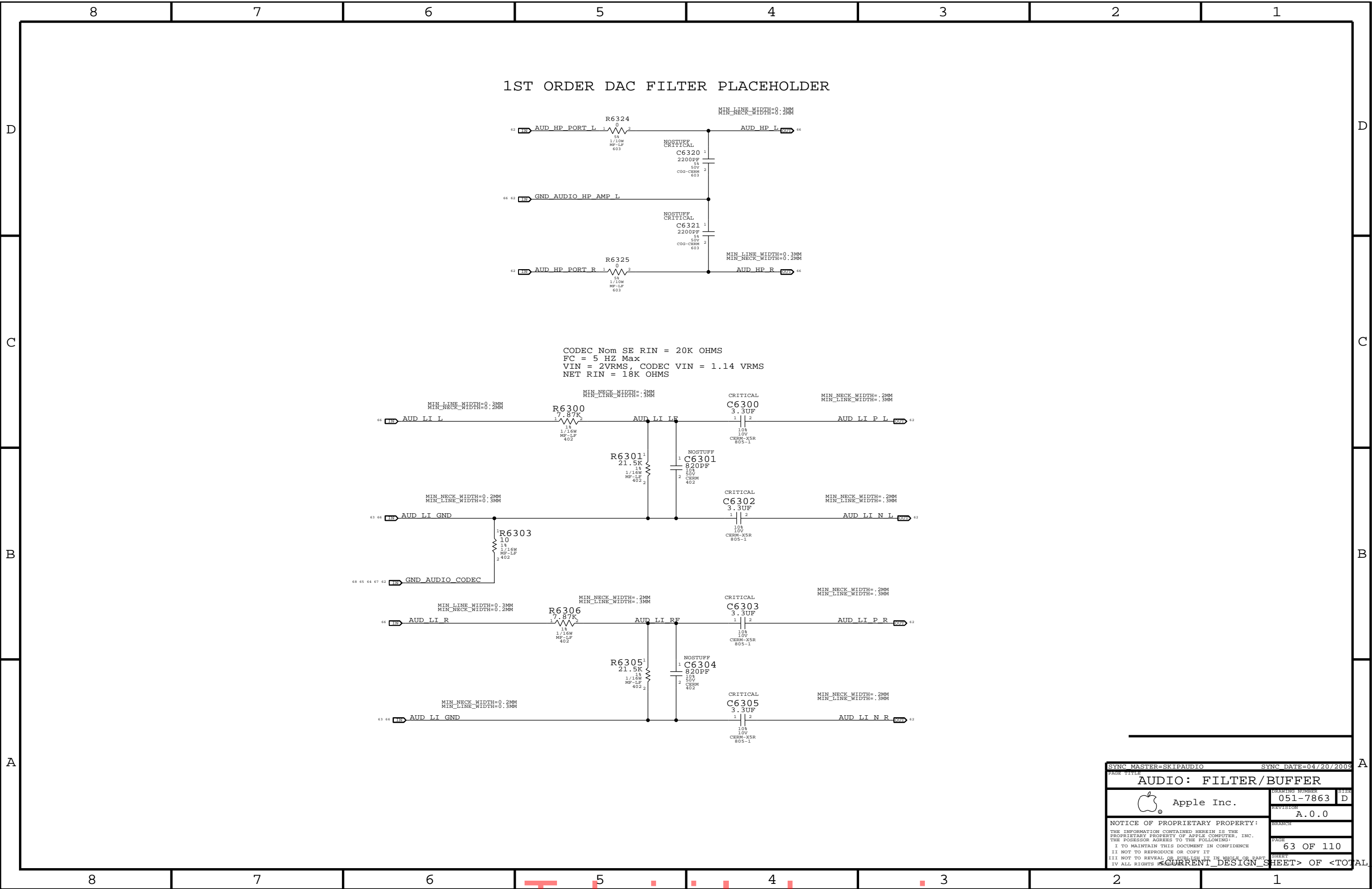
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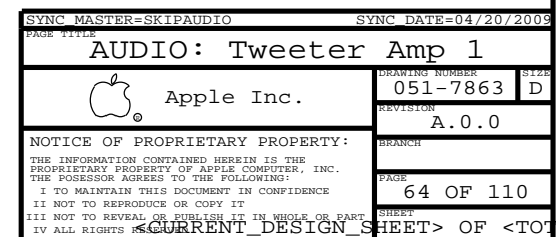
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```
GAIN = -4.8(20K/17.4K)    TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS     TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS      RIN = 17.4 OHMS
                           FC = 19.5 HZ
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N
```

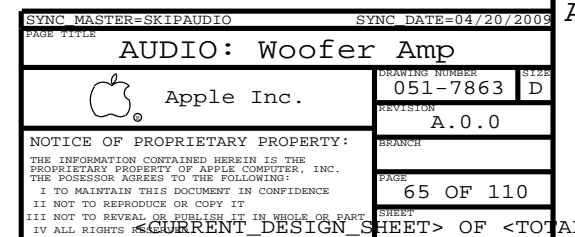


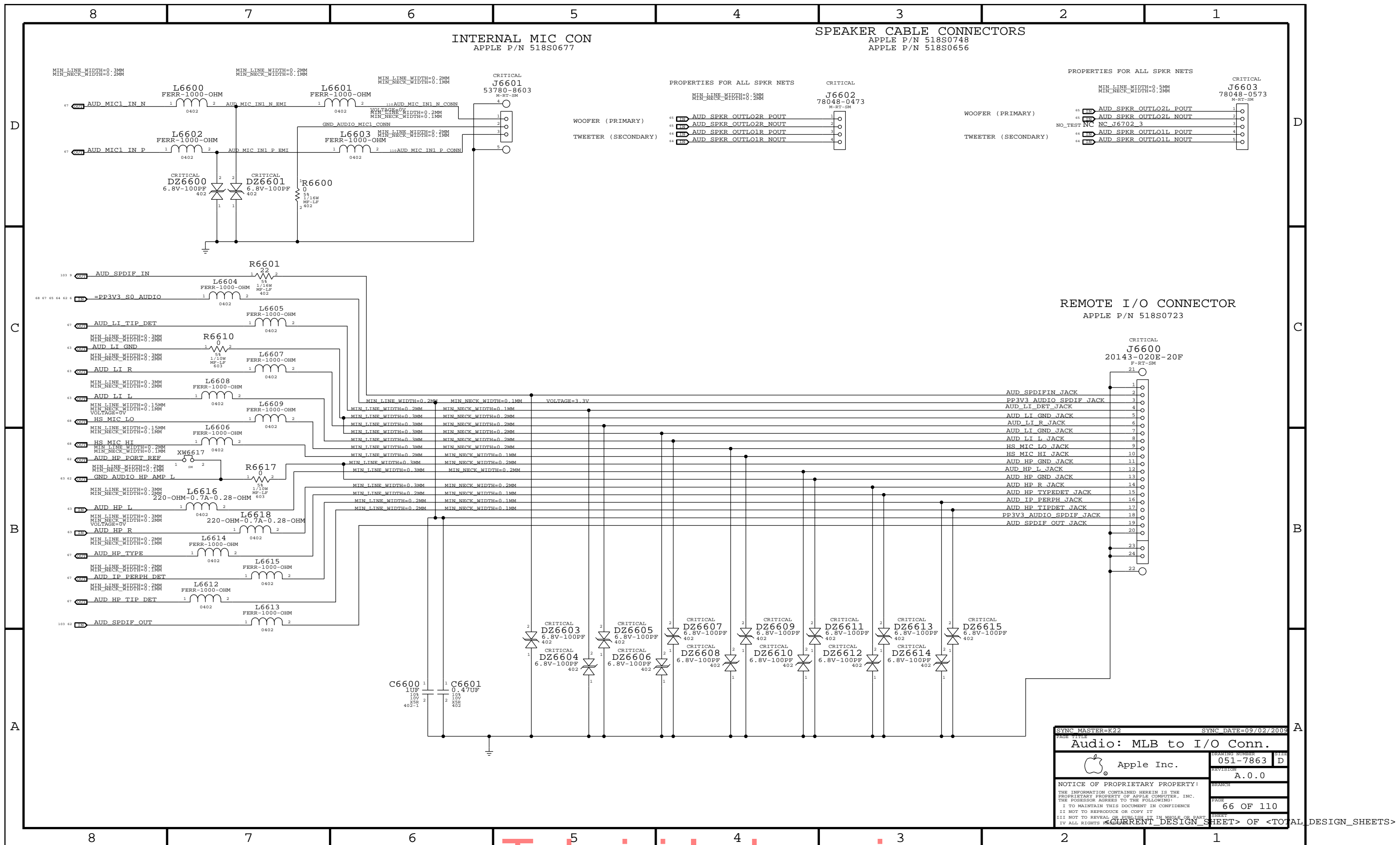
MAX9736B APN:353S2042

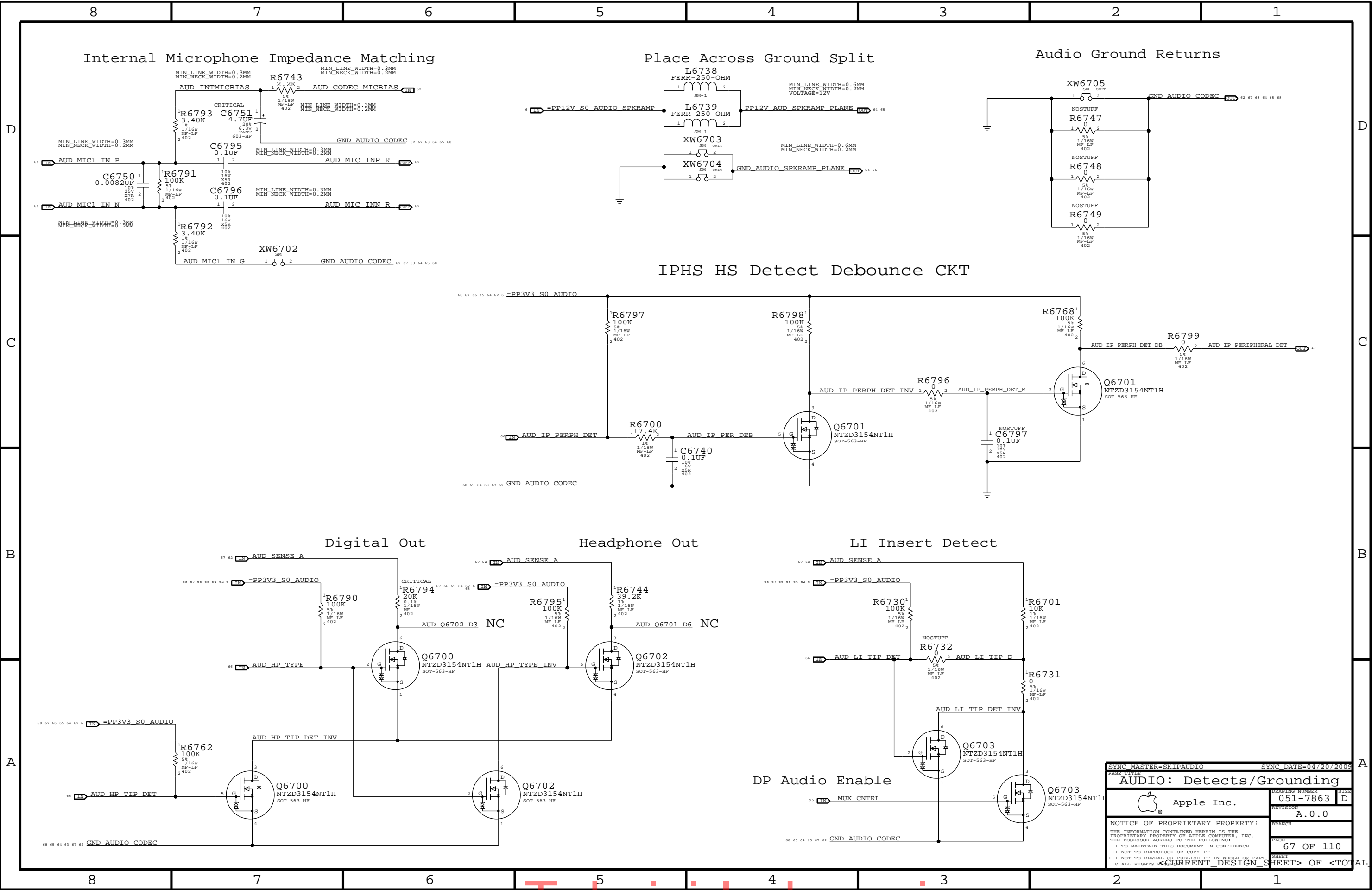
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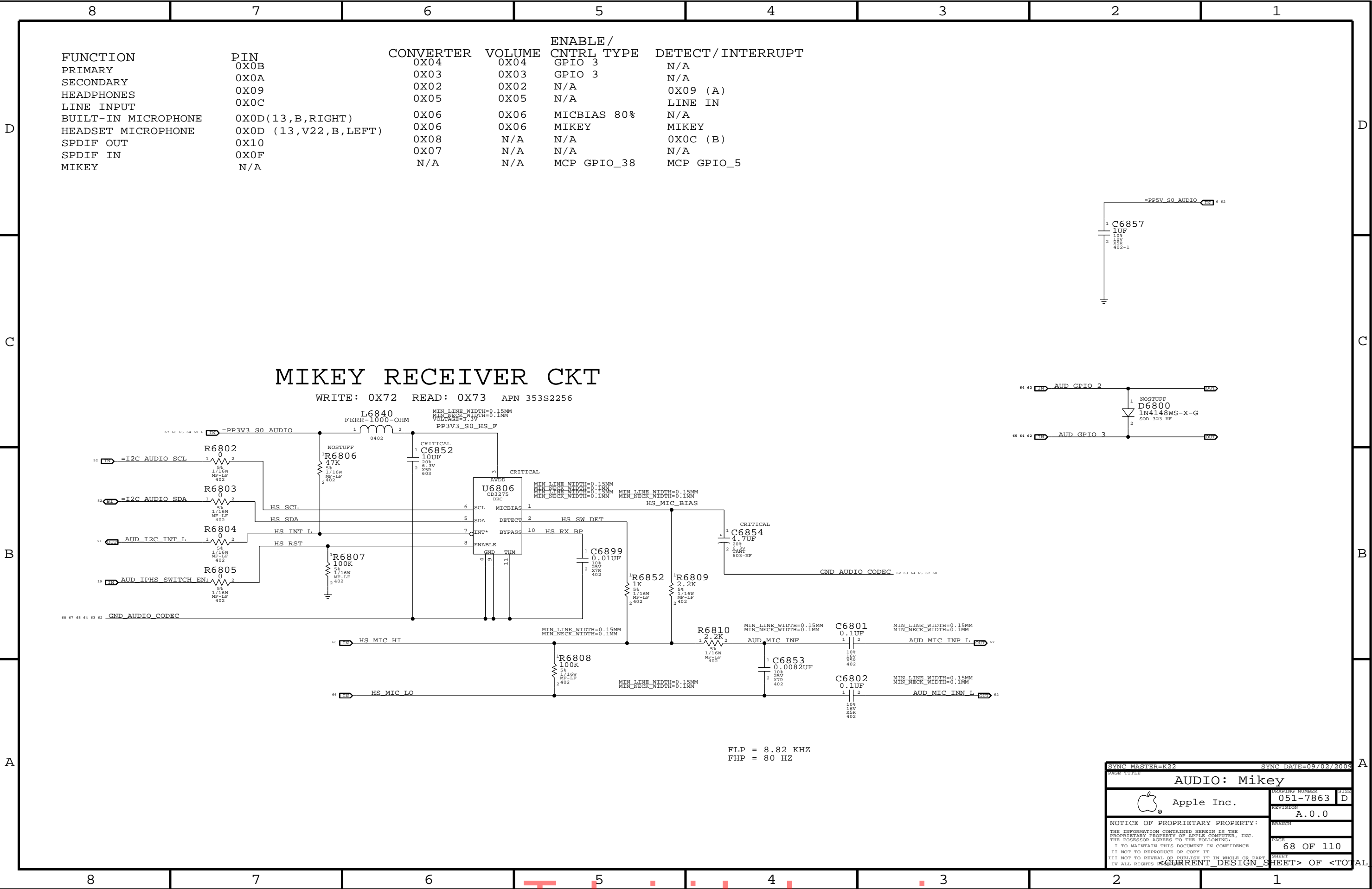
GAIN = -4.8(20K/17.4K)    TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS     TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS      RIN = 17.4 OHMS
POUT = 6.76 W INTO 8 OHMS FC = 19.5 HZ
                          @ 1% THD+N

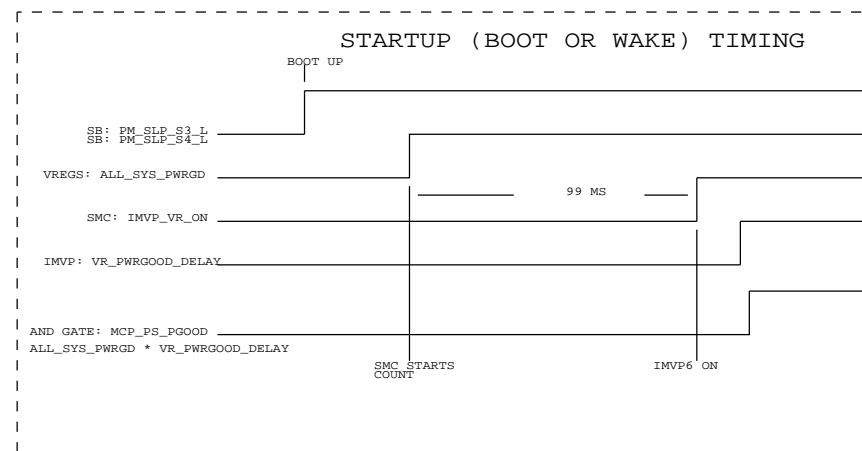
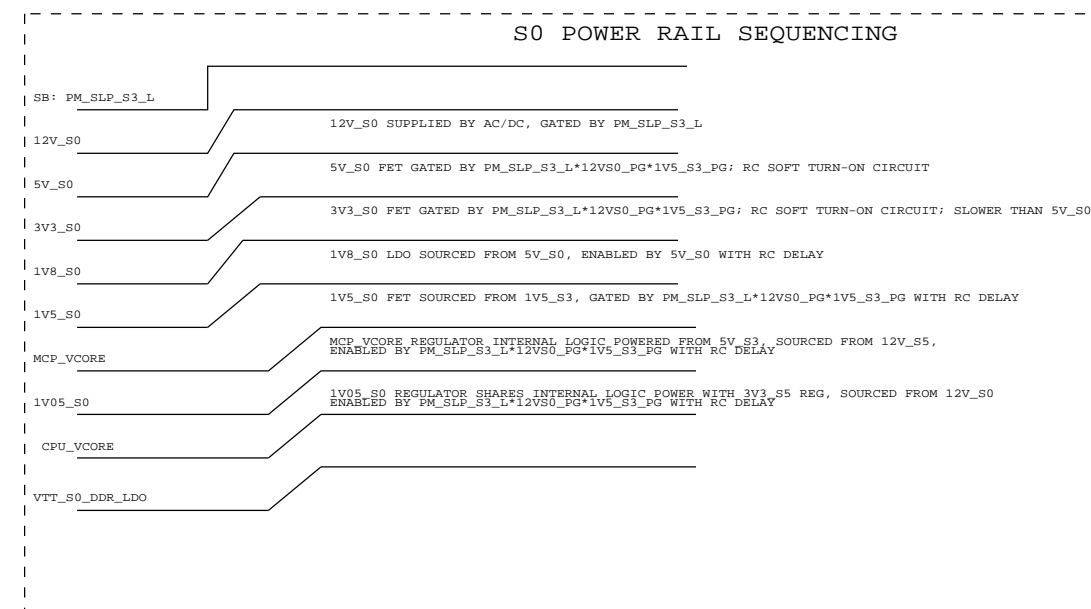
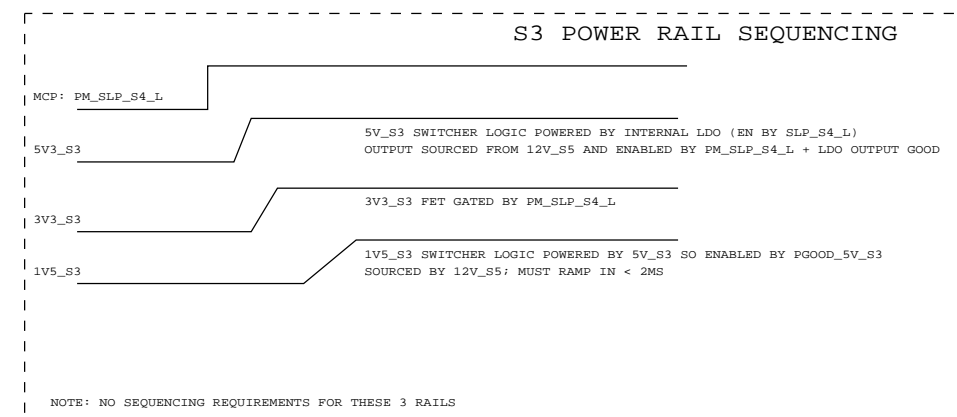
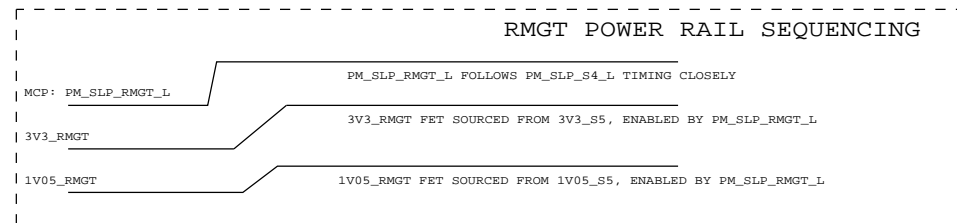
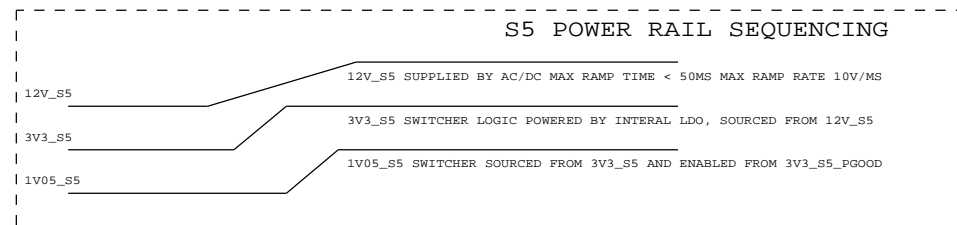
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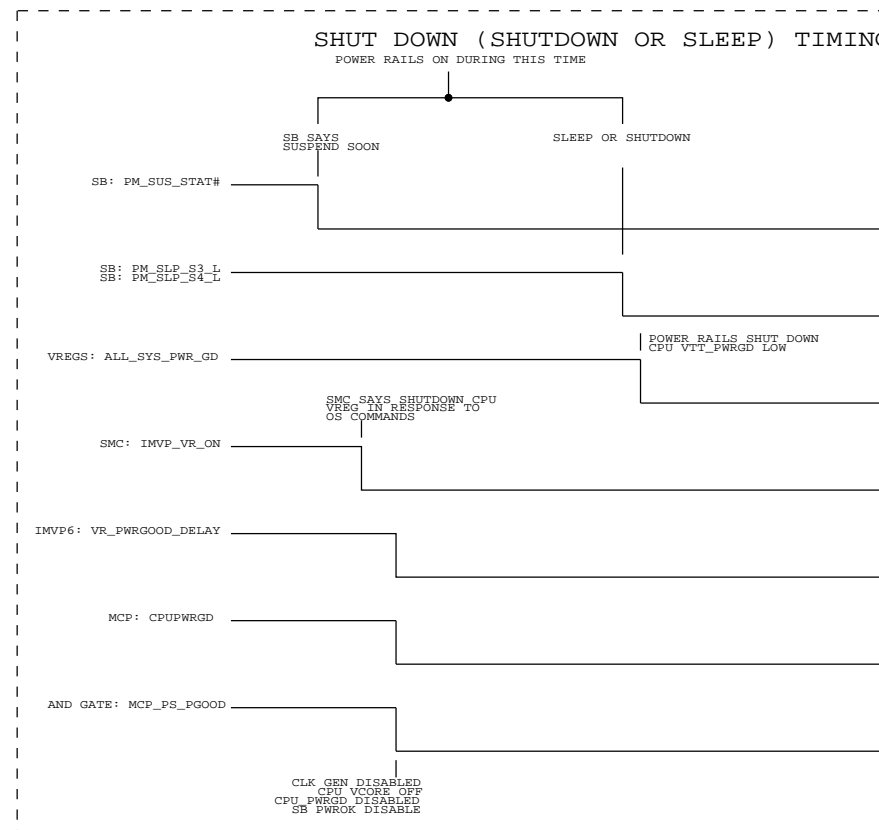


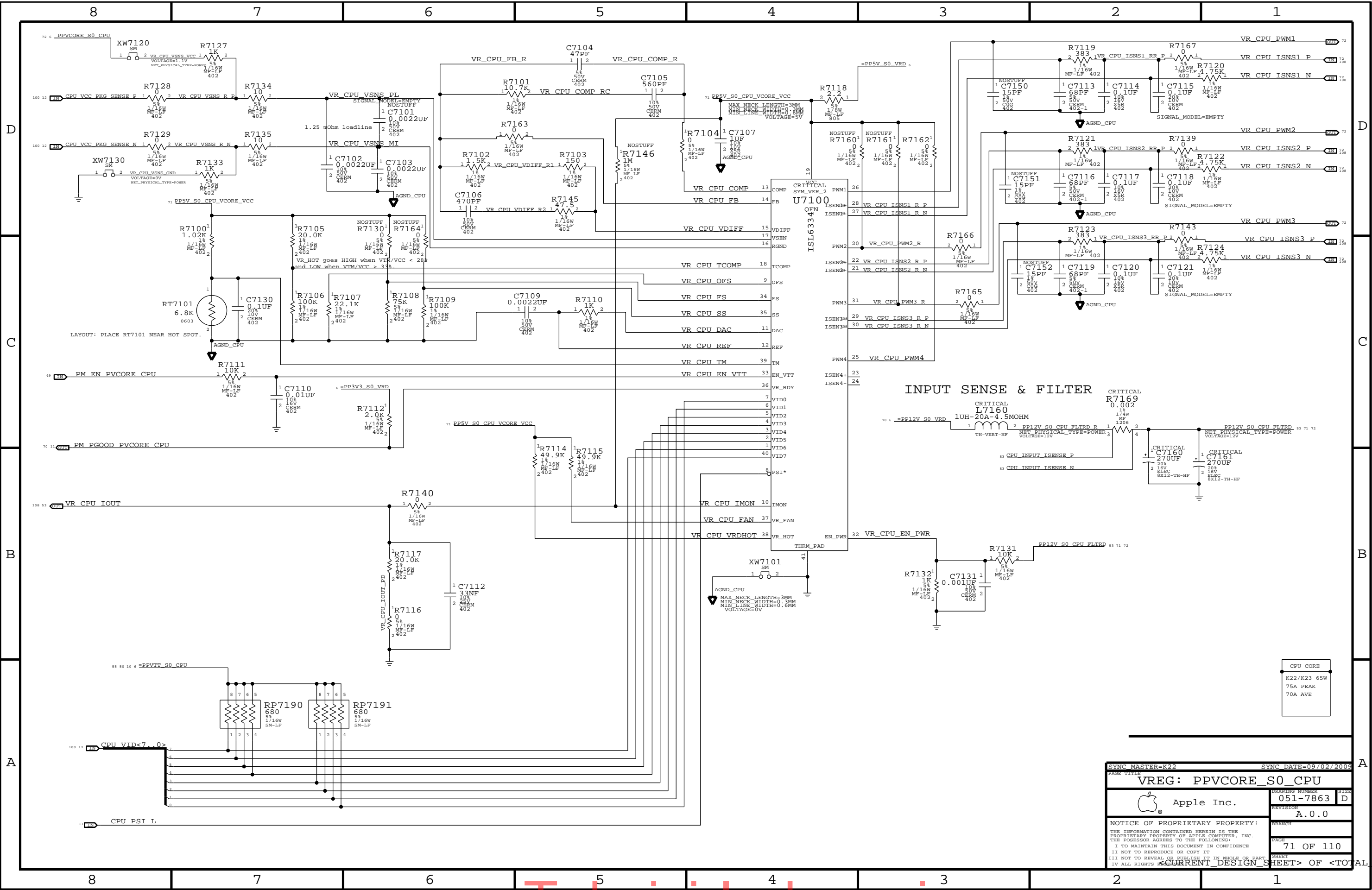




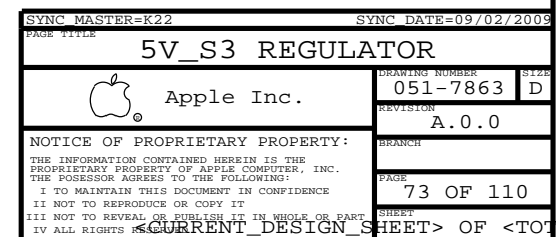


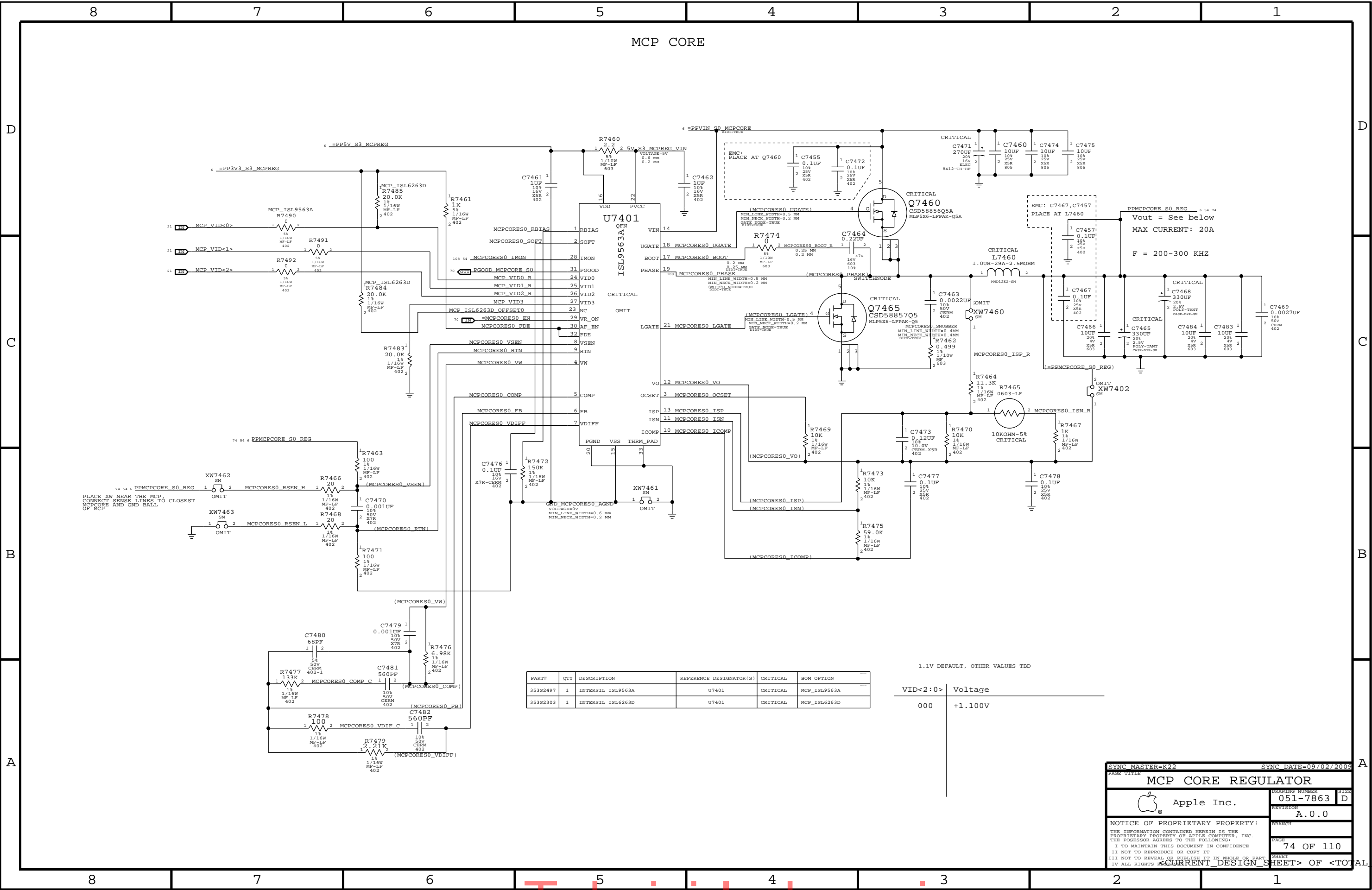
State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0



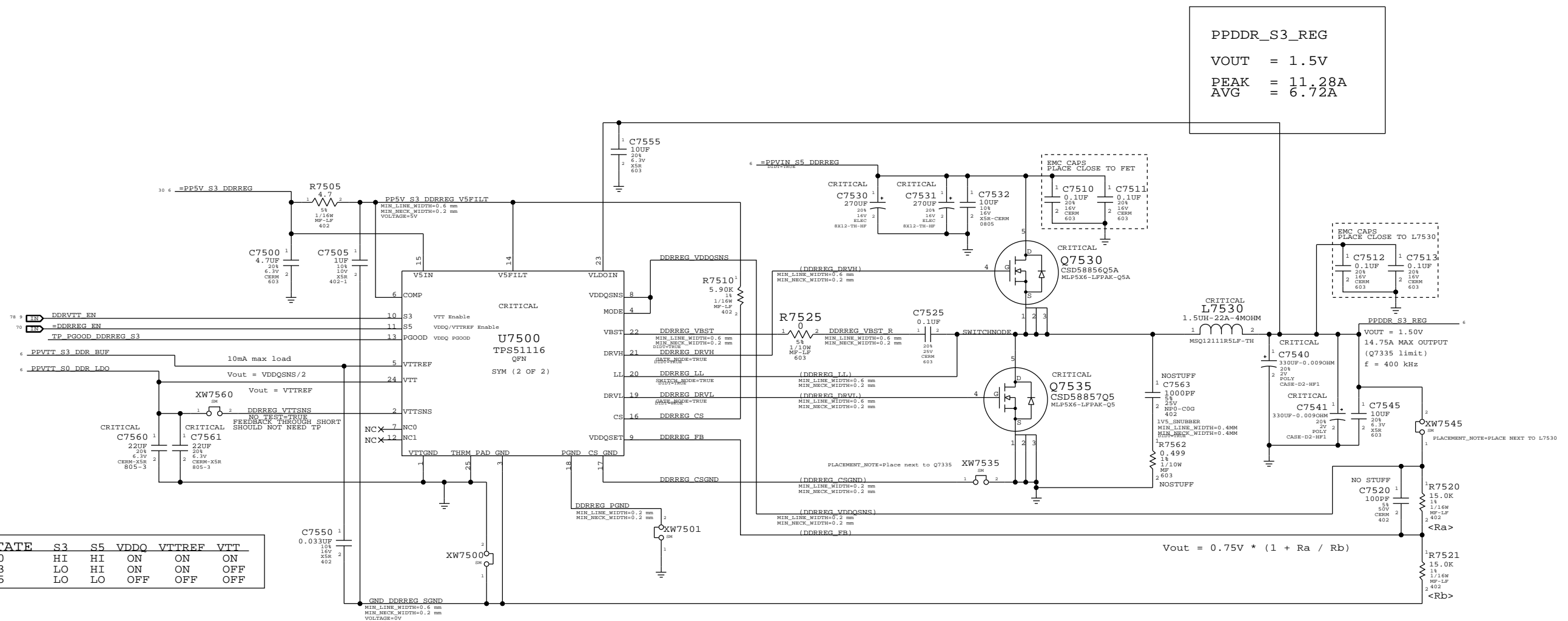


SYNC MASTER=K22		SYNC DATE=09/02/2009	
PAGE TITLE		PAGE	
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1.5 V DDR SUPPLY



PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11.28A
AVG = 6.72A

SYNC MASTER=K22

SYNC DATE=09/02/2009

1.5V DDR SUPPLY

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C									C
B									B
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MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.

IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY.


MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

A

	8	7	6	5	4	3	2	1	
D									D
C									C
B									B
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SYNC DATE=12/02/2008

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SYNC DATE=12/02/2008

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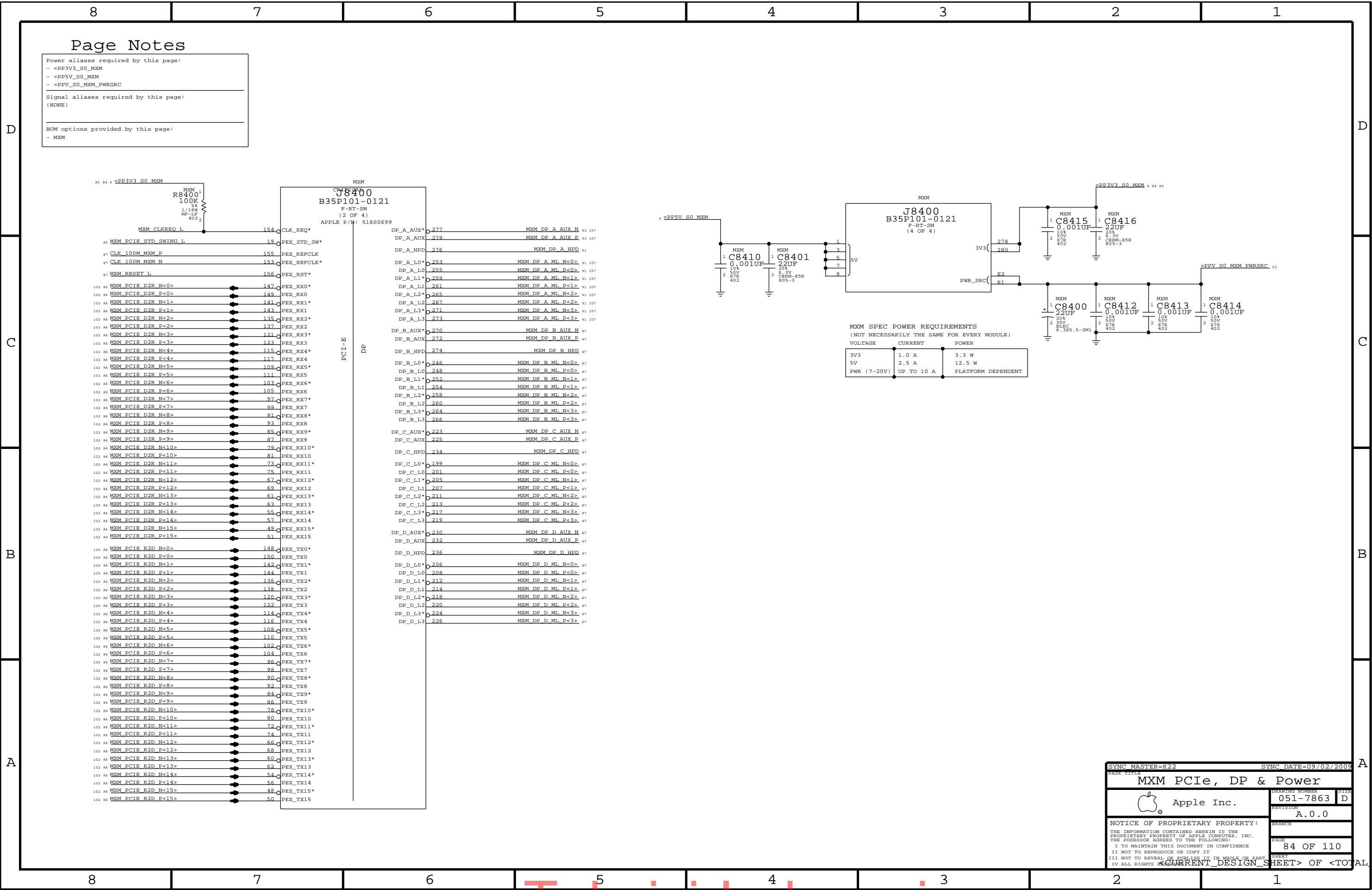
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Power aliases required by this page:

- =PP3V3_S0_MXM

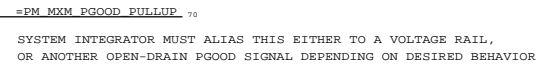
Signal aliases required by this page:

- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

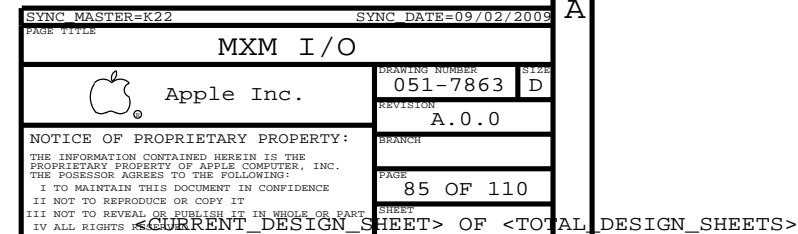
BOM options provided by this page:

FLOAT = NORMAL VGA MODE
 GND = SECONDARY DISPLAY CARD

FLOAT = LOW SWING
 GND = HIGH SWING



PLACE CLOSE TO J7800



8	7	6	5	4	3	2	1			
MXM TX CAPS				MXM RX CAPS						
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MXM PCIE CAPS

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MXM PCIE CAPS

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Page Notes

Power aliases required by this page:
~ =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP Connections

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84	CLK_100M_MXM_N	==	GPU_CLK100M_POIE_N	9 102
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18	LVDS_IG_A_DATA_P<3>	==	NC_LVDS_IG_A_DATA_P<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_A_DATA_N<3>	==	NC_LVDS_IG_A_DATA_N<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_CLK_P	==	NC_LVDS_IG_B_CLK_P	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_CLK_N	==	NC_LVDS_IG_B_CLK_N	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_P<0>	==	NC_LVDS_IG_B_DATA_P<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_N<0>	==	NC_LVDS_IG_B_DATA_N<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_P<1>	==	NC_LVDS_IG_B_DATA_P<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_N<1>	==	NC_LVDS_IG_B_DATA_N<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_P<2>	==	NC_LVDS_IG_B_DATA_P<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_N<2>	==	NC_LVDS_IG_B_DATA_N<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_P<3>	==	NC_LVDS_IG_B_DATA_P<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_B_DATA_N<3>	==	NC_LVDS_IG_B_DATA_N<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_DDC_CLK	==	NC_LVDS_IG_DDC_CLK	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_DDC_DATA	==	NC_LVDS_IG_DDC_DATA	
			MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MXM Interfaces

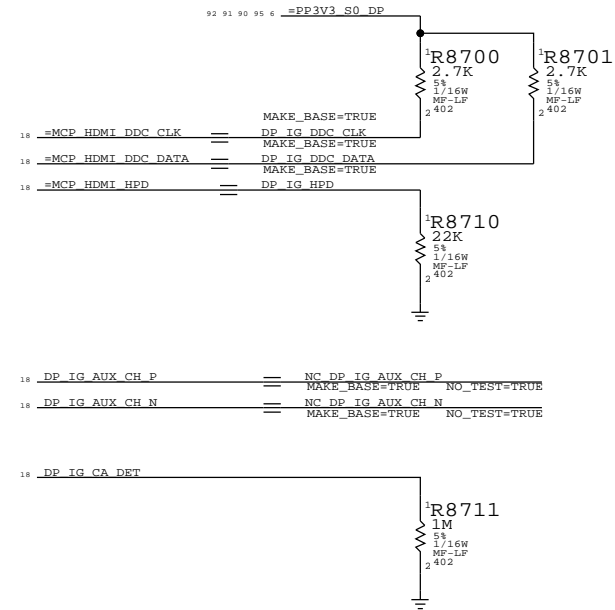
85	MXM_LVDS_A_CLK_N	==	NC_MXM_LVDS_A_CLK_N	
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			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_N<0>	==	NC_MXM_LVDS_A_DATA_N<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_P<0>	==	NC_MXM_LVDS_A_DATA_P<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_N<1>	==	NC_MXM_LVDS_A_DATA_N<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_P<1>	==	NC_MXM_LVDS_A_DATA_P<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_N<2>	==	NC_MXM_LVDS_A_DATA_N<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_P<2>	==	NC_MXM_LVDS_A_DATA_P<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_N<3>	==	NC_MXM_LVDS_A_DATA_N<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_A_DATA_P<3>	==	NC_MXM_LVDS_A_DATA_P<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_CLK_N	==	NC_MXM_LVDS_B_CLK_N	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_CLK_P	==	NC_MXM_LVDS_B_CLK_P	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_N<0>	==	NC_MXM_LVDS_B_DATA_N<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_P<0>	==	NC_MXM_LVDS_B_DATA_P<0>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_N<1>	==	NC_MXM_LVDS_B_DATA_N<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_P<1>	==	NC_MXM_LVDS_B_DATA_P<1>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_N<2>	==	NC_MXM_LVDS_B_DATA_N<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_P<2>	==	NC_MXM_LVDS_B_DATA_P<2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_N<3>	==	NC_MXM_LVDS_B_DATA_N<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM_LVDS_B_DATA_P<3>	==	NC_MXM_LVDS_B_DATA_P<3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MXM DP Interfaces

84	MXM_DP_B_MI_P<0..3>	==	NC_MXM_DP_B_MI_P<0..3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_B_MI_N<0..3>	==	NC_MXM_DP_B_MI_N<0..3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_B_AUX_P	==	NC_MXM_DP_B_AUX_P	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_B_AUX_N	==	NC_MXM_DP_B_AUX_N	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_B_HPD	==	NC_MXM_DP_B_HPD	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_D_MI_P<0..3>	==	NC_MXM_DP_D_MI_P<0..3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_D_MI_N<0..3>	==	NC_MXM_DP_D_MI_N<0..3>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_D_AUX_P	==	NC_MXM_DP_D_AUX_P	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_D_AUX_N	==	NC_MXM_DP_D_AUX_N	
			MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM_DP_D_HPD	==	NC_MXM_DP_D_HPD	
			MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MCP Interfaces

18	LVDS_IG_BKL_ON	==	NC_LVDS_IG_BKL_ON	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_BKL_PWM	==	NC_LVDS_IG_BKL_PWM	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS_IG_PANEL_FWR	==	NC_LVDS_IG_PANEL_FWR	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	=MCP_HDMI_TXD_P<0..2>	==	NC_MCP_HDMI_TXD_P<0..2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	=MCP_HDMI_TXD_N<0..2>	==	NC_MCP_HDMI_TXD_N<0..2>	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	=MCP_HDMI_TXC_P	==	NC_MCP_HDMI_TXC_P	
			MAKE_BASE=TRUE	NO_TEST=TRUE
18	=MCP_HDMI_TXC_N	==	NC_MCP_HDMI_TXC_N	
			MAKE_BASE=TRUE	NO_TEST=TRUE



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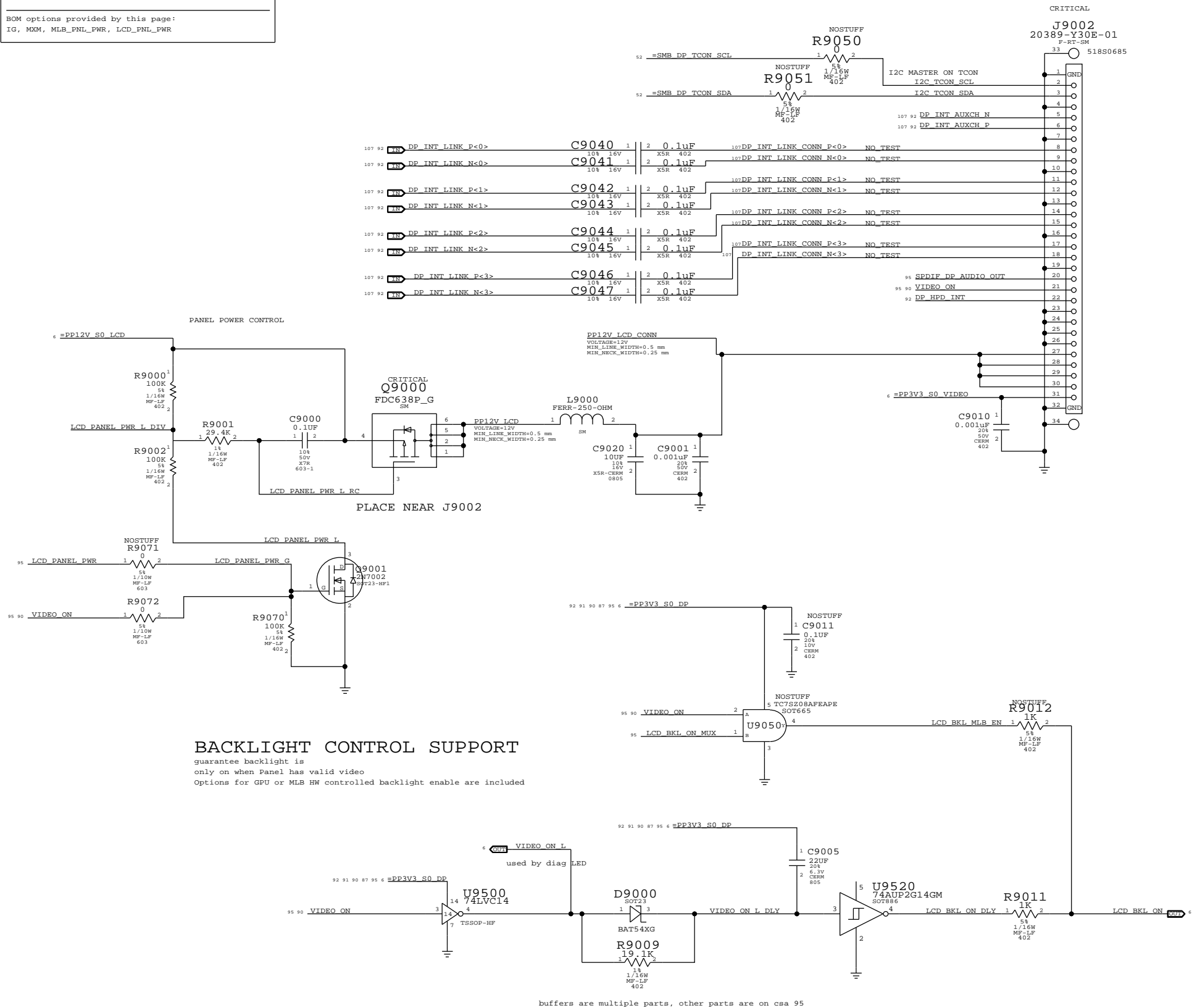
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- =PP3V3_S0_VIDEO

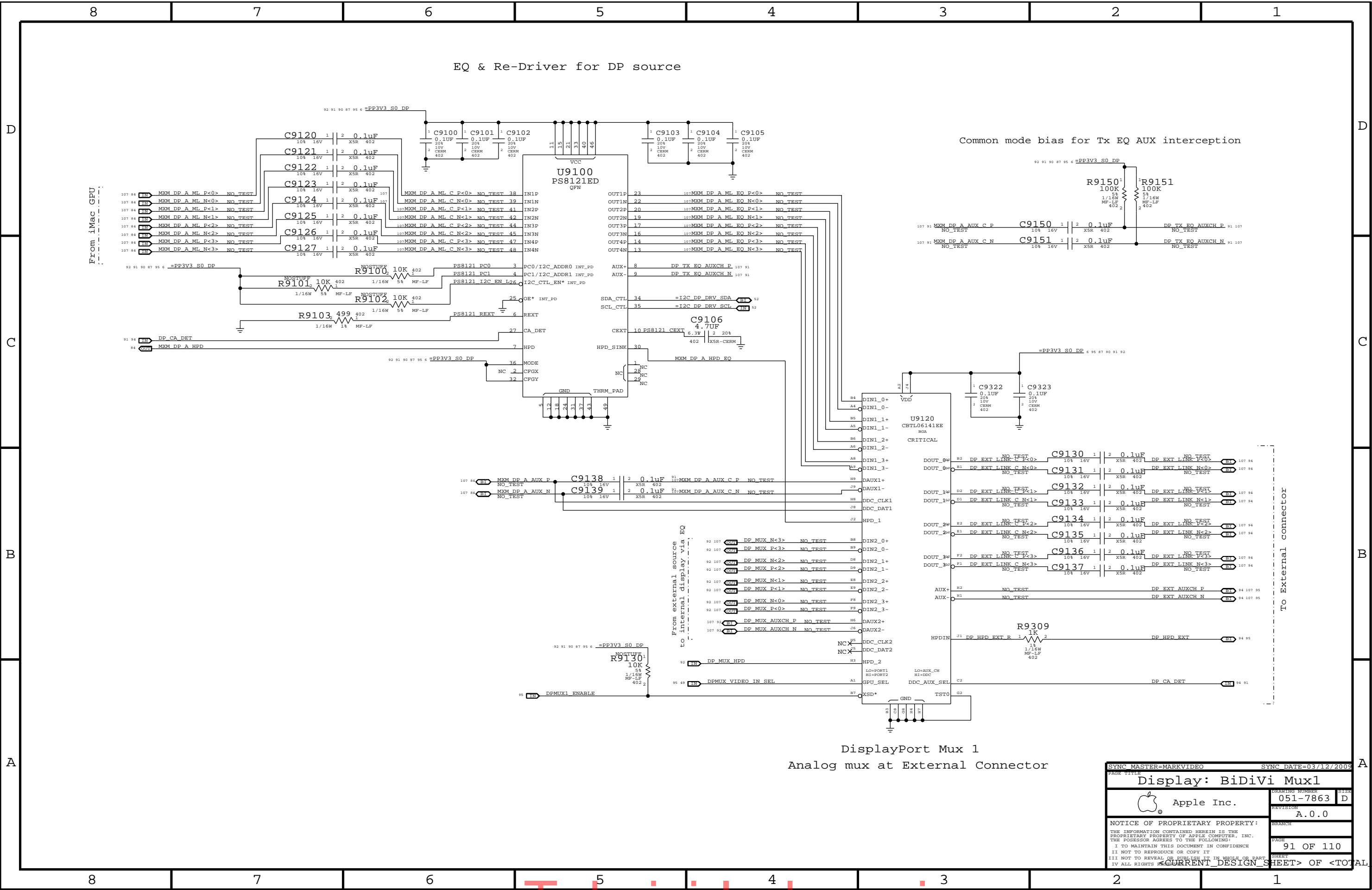
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BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

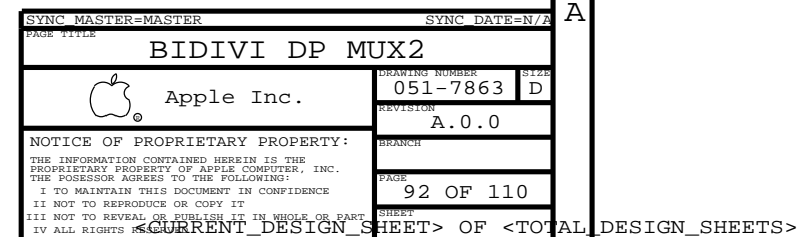
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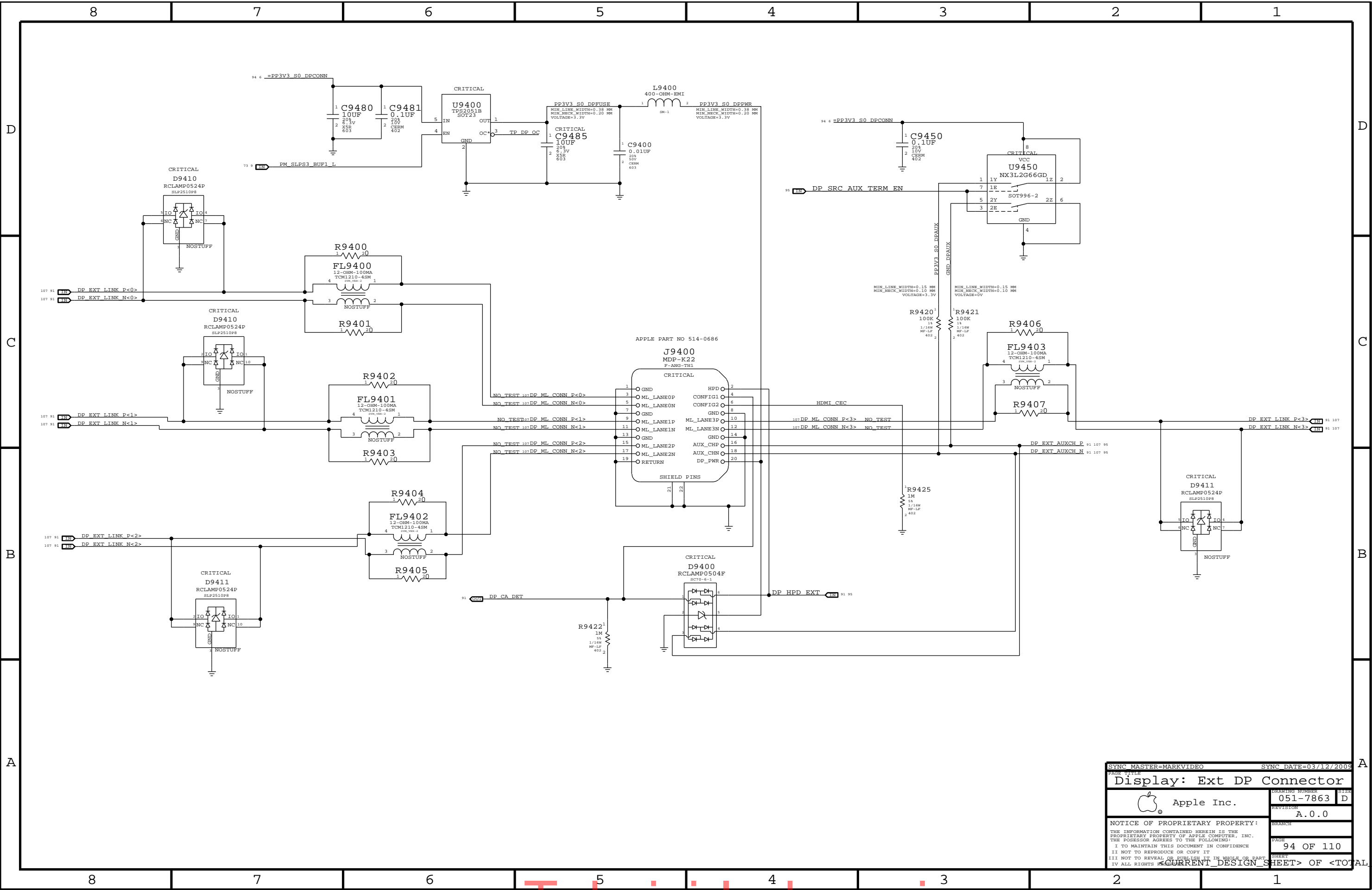



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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4x signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighter than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.
Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SMIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET

PHYSICAL

SPACING

Group 0

FSB_42S

FSB_DATA

FSB D L<15..0>

10 14

Group 1

FSB_42S

FSB_DATA

FSB DINV L<0>

10 14

Group 2

FSB_42S

FSB_DATA

FSB D L<31..16>

10 14

Group 3

FSB_42S

FSB_DATA

FSB DINV L<1>

10 14

Group 0

FSB_42S

FSB_DATA

FSB DSTB L P<0>

10 14

Group 1

FSB_42S

FSB_DATA

FSB DSTB L N<0>

10 14

Group 2

FSB_42S

FSB_DATA

FSB D L<47..32>

10 14

Group 3

FSB_42S

FSB_DATA

FSB DINV L<2>

10 14

Group 0

FSB_42S

FSB_DATA

FSB DSTB L P<1>

10 14

Group 1

FSB_42S

FSB_DATA

FSB DSTB L N<1>

10 14

Group 2

FSB_42S

FSB_DATA

FSB D L<63..48>

10 14

Group 3

FSB_42S

FSB_DATA

FSB DINV L<3>

10 14

Group 0

FSB_42S

FSB_DATA

FSB DSTB L P<3>

10 14

Group 1

FSB_42S

FSB_DATA

FSB DSTB L N<3>

10 14

Group 0

FSB_50S

FSB_ADDR

FSB A L<16..3>

10 14

Group 1

FSB_50S

FSB_ADDR

FSB REQ L<4..0>

10 14

Group 2

FSB_50S

FSB_ADDR

FSB ADSTB L<0>

10 14

Group 3

FSB_50S

FSB_ADDR

FSB A L<35..17>

10 14

Group 4

FSB_50S

FSB_ADDR

FSB ADSTB L<1>

10 14

Group 5

FSB_50S

FSB_ADDR

FSB ADS L

10 14

Group 6

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 7

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 8

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 9

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 10

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 11

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 12

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 13

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 14

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 15

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 16

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 17

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 18

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 19

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 20

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 21

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 22

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 23

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 24

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 25

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 26

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 27

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 28

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 29

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 30

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 31

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 32

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 33

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 34

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 35

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 36

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 37

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 38

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 39

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 40

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 41

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 42

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 43

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 44

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 45

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 46

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 47

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 48

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 49

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 50

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 51

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 52

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 53

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 54

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 55

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 56

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 57

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 58

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 59

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 60

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 61

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 62

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 63

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 64

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 65

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 66

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 67

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 68

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 69

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 70

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 71

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 72

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 73

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 74

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 75

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 76

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 77

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 78

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 79

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 80

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 81

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 82

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 83

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 84

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 85

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 86

FSB_50S

FSB_ADDR

FSB BNR L

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Group 87

FSB_50S

FSB_ADDR

FSB BPRI L

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Group 88

FSB_50S

FSB_ADDR

FSB DBSY L

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Group 89

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 90

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 91

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 92

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 93

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 94

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 95

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 96

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 97

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 98

FSB_50S

FSB_ADDR

FSB BREQ1 L

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Group 99

FSB_50S

FSB_ADDR

FSB BNR L

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Group 100

FSB_50S

FSB_ADDR

FSB BPRI L

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Group 101

FSB_50S

FSB_ADDR

FSB DBSY L

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Group 102

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 103

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 104

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 105

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 106

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 107

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 108

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 109

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 110

FSB_50S

FSB_ADDR

FSB BREQ0 L

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Group 111

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 112

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 113

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 114

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 115

FSB_50S

FSB_ADDR

FSB DEFER L

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Group 116

FSB_50S

FSB_ADDR

FSB DEDY L

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Group 117

FSB_50S

FSB_ADDR

FSB HIT L

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Group 118

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 119

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 120

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 121

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 122

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 123

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 124

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 125

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 126

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 127

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 128

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 129

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 130

FSB_50S

FSB_ADDR

FSB HIT L

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Group 131

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 132

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 133

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 134

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 135

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 136

FSB_50S

FSB_ADDR

FSB BREQ0 L

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Group 137

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 138

FSB_50S

FSB_ADDR

FSB BNR L

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Group 139

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 140

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 141

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 142

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 143

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 144

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 145

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 146

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 147

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 148

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 149

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 150

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 151

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 152

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 153

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 154

FSB_50S

FSB_ADDR

FSB DEFER L

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Group 155

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

Group 156

FSB_50S

FSB_ADDR

FSB HIT L

10 14

Group 157

FSB_50S

FSB_ADDR

FSB HITM L

10 14

Group 158

FSB_50S

FSB_ADDR

FSB LOCK L

10 14

Group 159

FSB_50S

FSB_ADDR

FSB CPURST L

10 13 14

Group 160

FSB_50S

FSB_ADDR

FSB RS L<2..0>

10 14

Group 161

FSB_50S

FSB_ADDR

FSB TRDY L

10 14

Group 162

FSB_50S

FSB_ADDR

FSB BREQ0 L

10 14

Group 163

FSB_50S

FSB_ADDR

FSB BREQ1 L

10 14

Group 164

FSB_50S

FSB_ADDR

FSB BNR L

10 14

Group 165

FSB_50S

FSB_ADDR

FSB BPRI L

10 14

Group 166

FSB_50S

FSB_ADDR

FSB DBSY L

10 14

Group 167

FSB_50S

FSB_ADDR

FSB DEFER L

10 14

Group 168

FSB_50S

FSB_ADDR

FSB DEDY L

10 14

8

7

6

5

4

3

2

1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4QS		=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_4QS_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM.*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MEM_70D_VDD	MEM_CLK	MEM A CLK P<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM A CLK N<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM A CLK P<4..3>	16 33
MEM_70D_VDD	MEM_CLK	MEM A CLK N<4..3>	16 33
MEM_4QS_VDD	MEM_CTRL	MEM A CKE<3..0>	15 16 31
MEM_4QS_VDD	MEM_CTRL	MEM A CS L<3..0>	15 16 31
MEM_4QS_VDD	MEM_CTRL	MEM A ODT<3..0>	15 16 31
MEM_4QS_VDD	MEM_CMD	MEM A A<14..0>	15 31
MEM_4QS_VDD	MEM_CMD	MEM A BA<2..0>	15 31
MEM_4QS_VDD	MEM_CMD	MEM A RAS L	15 31
MEM_4QS_VDD	MEM_CMD	MEM A CAS L	15 31
MEM_4QS_VDD	MEM_CMD	MEM A WE L	15 31
MEM_4QS	MEM_DATA	MEM A DQ<7..0>	15 33
MEM_4QS	MEM_DATA	MEM A DM<0>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<15..8>	15 33
MEM_4QS	MEM_DATA	MEM A DM<1>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<23..16>	15 33
MEM_4QS	MEM_DATA	MEM A DM<2>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<31..24>	15 33
MEM_4QS	MEM_DATA	MEM A DM<3>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<39..32>	15 33
MEM_4QS	MEM_DATA	MEM A DM<4>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<47..40>	15 33
MEM_4QS	MEM_DATA	MEM A DM<5>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<55..48>	15 33
MEM_4QS	MEM_DATA	MEM A DM<6>	15 33
MEM_4QS	MEM_DATA	MEM A DQ<63..56>	15 33
MEM_4QS	MEM_DATA	MEM A DM<7>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<0>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<0>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<1>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<1>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<2>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<2>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<3>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<3>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<4>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<4>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<5>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<5>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<6>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<6>	15 33
MEM_70D	MEM_DQS	MEM A DQS P<7>	15 33
MEM_70D	MEM_DQS	MEM A DQS N<7>	15 33
MEM_70D_VDD	MEM_CLK	MEM B CLK P<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM B CLK N<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM B CLK P<4..3>	16 33
MEM_70D_VDD	MEM_CLK	MEM B CLK N<4..3>	16 33
MEM_4QS_VDD	MEM_CTRL	MEM B CKE<3..0>	15 16 32
MEM_4QS_VDD	MEM_CTRL	MEM B CS L<3..0>	15 16 32
MEM_4QS_VDD	MEM_CTRL	MEM B ODT<3..0>	15 16 32
MEM_4QS_VDD	MEM_CMD	MEM B A<14..0>	15 32
MEM_4QS_VDD	MEM_CMD	MEM B BA<2..0>	15 32
MEM_4QS_VDD	MEM_CMD	MEM B RAS L	15 32
MEM_4QS_VDD	MEM_CMD	MEM B CAS L	15 32
MEM_4QS_VDD	MEM_CMD	MEM B WE L	15 32
MEM_4QS	MEM_DATA	MEM B DQ<7..0>	15 33
MEM_4QS	MEM_DATA	MEM B DM<0>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<15..8>	15 33
MEM_4QS	MEM_DATA	MEM B DM<1>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<23..16>	15 33
MEM_4QS	MEM_DATA	MEM B DM<2>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<31..24>	15 33
MEM_4QS	MEM_DATA	MEM B DM<3>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<39..32>	15 33
MEM_4QS	MEM_DATA	MEM B DM<4>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<47..40>	15 33
MEM_4QS	MEM_DATA	MEM B DM<5>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<55..48>	15 33
MEM_4QS	MEM_DATA	MEM B DM<6>	15 33
MEM_4QS	MEM_DATA	MEM B DQ<63..56>	15 33
MEM_4QS	MEM_DATA	MEM B DM<7>	15 33
MEM_70D_VDD	MEM_CLK	MEM B CLK P<0>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<0>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<1>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<1>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<2>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<2>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<3>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<3>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<4>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<4>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<5>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<5>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<6>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<6>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS P<7>	15 33
MEM_70D_VDD	MEM_CLK	MEM B DQS N<7>	15 33
MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MEM_70D_VDD	MEM_DQS	MEM B DQS P<0>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<0>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<1>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<1>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<2>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<2>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<3>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<3>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<4>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<4>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<5>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<5>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<6>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<6>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS P<7>	15 33
MEM_70D_VDD	MEM_DQS	MEM B DQS N<7>	15 33
MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

SYNC MASTER=K22

SYNC DATE=09/02/2009

Memory Constraints

Apple Inc.

051-7863

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34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D N 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D C P 17 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D C N 17 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D L P 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D L N 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI D2R P 17 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI D2R N 17 34</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW R2D P 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW R2D N 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW R2D C P 17 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW R2D C N 17 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW D2R P 17 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW D2R N 17 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW D2R C P 41</td></tr><tr><td></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FW D2R C N 41</td></tr><tr><td colspan="4">PCIE REF CLOCKS</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>GPU CLK100M PCIE P 9 87</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>GPU CLK100M PCIE N 9 87</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI P 17 34</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI N 17 34</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI CON P 34</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI CON N 34</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M FW P 17 41</td></tr><tr><td></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M FW N 17 41</td></tr><tr><td colspan="4">SATA</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD R2D C P 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD R2D C N 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD R2D P 45 110</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD R2D N 45 110</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD D2R P 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD D2R N 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD D2R C P 45 110</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA HDD D2R C N 45 110</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA ODD R2D C P 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA ODD R2D C N 20 45</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA ODD R2D P 45 110</td></tr><tr><td></td><td>SATA_100D</td><td>SATA</td><td>SATA ODD R2D N 45 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34		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N 17 34		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CON P 34		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CON N 34		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P 17 41		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N 17 41	SATA					SATA_100D	SATA	SATA HDD R2D C P 20 45		SATA_100D	SATA	SATA HDD R2D C N 20 45		SATA_100D	SATA	SATA HDD R2D P 45 110		SATA_100D	SATA	SATA HDD R2D N 45 110		SATA_100D	SATA	SATA HDD D2R P 20 45		SATA_100D	SATA	SATA HDD D2R N 20 45		SATA_100D	SATA	SATA HDD D2R C P 45 110		SATA_100D	SATA	SATA HDD D2R C N 45 110		SATA_100D	SATA	SATA ODD R2D C P 20 45		SATA_100D	SATA	SATA ODD R2D C N 20 45		SATA_100D	SATA	SATA ODD R2D P 45 110		SATA_100D	SATA	SATA ODD R2D N 45 110		SATA_100D	SATA	SATA ODD D2R P 20 45		SATA_100D	SATA	SATA ODD D2R N 20 45		SATA_100D	SATA	SATA ODD D2R C P 45 110		SATA_100D	SATA	SATA ODD D2R C N 45 110		MCP_50S	SATA_TERM	MCP SATA_TERM 20	MISC					MCP_50S	MCP_PEX_COMP	MCP_PEX_CLK_COMP 17		MCP_FW_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET 18 26		MCP_50S	MCP_PEX_COMP	MCP_IFPAB_VPROBE 18 26				PM_SLP_S3_L 9 21				PM_SLP_S4_L 21 70
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	MCP_FW_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET 18 26																																																																																																																																																																																																																																																							
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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4K_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCI_55S	PCI	PCI REQ0 L	19
	PCI_55S	PCI	PCI REQ1 L	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP	19
	LPC_55S	LPC	LPC AD<3...0>	19 49 51
	LPC_55S	LPC	LPC AD R<3...0>	19
	LPC_55S	LPC	LPC FRAME L	19 49 51
	LPC_55S	LPC	LPC FRAME R L	19
	LPC_55S	LPC	LPC RESET L	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	9 49
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	9 51
	CLK_LPC_55S	CLK_LPC	PM_CLK32K SUSCLK_R	9 21
	CLK_LPC_55S	CLK_LPC	PM_CLK32K SUSCLK	9 49
	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	20
	USB_90D	USB	USB_EXT_A_P	20 46
	USB_90D	USB	USB_EXT_A_N	20 46
	USB_90D	USB	USB_PORT0_P	46
	USB_90D	USB	USB_PORT0_N	46
	USB_90D	USB	USB_EXT_B_P	20 46
	USB_90D	USB	USB_EXT_B_N	20 46
	USB_90D	USB	USB_PORT1_P	46
	USB_90D	USB	USB_PORT1_N	46
	USB_90D	USB	USB_EXT_C_P	20 46
	USB_90D	USB	USB_EXT_C_N	20 46
	USB_90D	USB	USB_PORT2_P	46
	USB_90D	USB	USB_PORT2_N	46
	USB_90D	USB	USB_EXT_D_P	20 46
	USB_90D	USB	USB_EXT_D_N	20 46
	USB_90D	USB	USB_D_MUXED_P	46
	USB_90D	USB	USB_D_MUXED_N	46
	USB_90D	USB	USB_PORT3_P	46
	USB_90D	USB	USB_PORT3_N	46
	USB_90D	USB	USB_CAMERA_P	20 47
	USB_90D	USB	USB_CAMERA_N	20 47
	USB_90D	USB	USB_CAMERA_L_P	47 110
	USB_90D	USB	USB_CAMERA_L_N	47 110
	USB_90D	USB	USB_BT_P	20 47
	USB_90D	USB	USB_BT_N	20 47
	USB_90D	USB	USB_BT_L_P	47 110
	USB_90D	USB	USB_BT_L_N	47 110
	USB_90D	USB	USB_IR_P	20 47
	USB_90D	USB	USB_IR_N	20 47
	USB_90D	USB	USB_IR_L_P	47 110
	USB_90D	USB	USB_IR_L_N	47 110
	USB_90D	USB	USB_SDCARD_P	20 47
	USB_90D	USB	USB_SDCARD_N	20 47
	USB_90D	USB	USB_SDCARD_L_P	47 110
	USB_90D	USB	USB_SDCARD_L_N	47 110
	MCP_55S	SPI	SPI_CLK_R	21 51 61
	MCP_55S	SPI	SPI_CLK	61
	MCP_55S	SPI	SPI_MOSI_R	21 51 61
	MCP_55S	SPI	SPI_MOSI	61
	MCP_55S	SPI	SPI_MISO	21 51 61
	MCP_55S	SPI	SPI_MISO_R	61
	MCP_55S	SPI	SPI_CS0_R_L	21 51
	MCP_55S	SPI	SPI_CS0_L	51
	HDA_55S	HDA	HDA_BIT_CLK	21 62
	MCP_HDA_PULLDN_COMP		MCP_HDA_PULLDN_COMP	21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
	HDA_55S	HDA	HDA_RST_L	21 62
	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_SDOUT	21 62
	HDA_55S	HDA	HDA_SDOUT_R	21
	HDA_55S	HDA	HDA_SYNC	21 62
	HDA_55S	HDA	HDA_SYNC_R	21
	HDA_55S	HDA	HDA_SDIN0	21 62
	HDA_55S	HDA	AUD_SDI_R	62
		HDA	AUD_SPDIF_IN	9 66
		HDA	AUD_SPDIF_OUT	62 66
		HDA	AUD_SPDIF_CHIP	62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	21 28

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SYNC DATE=09/02/2009

MCP Constraints 2

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
	FW_110D	FW_TP
	FW_110D	FW_TP
	FW_110D	FW_TP
	FW_110D	FW_TP
PORT 1 & 2 NOT USED		
	FW_110D	FW_TP
	FW_110D	FW_TP
	FW_110D	FW_TP
	FW_110D	FW_TP

FireWire Constraints

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_OTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALT. ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	350 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE		SPACING		
		FRONT MEM		=P1V5 S3 MEM A	6	30 31
		FRONT MEM		=P1V5 S3 MEM B	6	30 32
		SWITCHNODE		VR CPU SW1	72	
		SWITCHNODE		VR CPU SW2	72	
		SWITCHNODE		VR CPU SW3	72	
		SWITCHNODE		1V8 SW	80	
		SWITCHNODE		1V1S5 SW	79	
		SWITCHNODE		PVTS0 PHASE	76	
		SWITCHNODE		3V3S5 SW	76	
		SWITCHNODE		5V83 SW	73	
		SWITCHNODE		MPCORES0 PHASE	74	
		THERM DIFF	THERMAL	SNS T DP1 DN6	55	
		THERM DIFF	THERMAL	SNS T DN1 DP6	55	
		THERM DIFF	THERMAL	SNS T DP2 DN3	55	
		THERM DIFF	THERMAL	SNS T DN2 DP3	55	
		THERM DIFF	THERMAL	CPU THERMD P	11	55
		THERM DIFF	THERMAL	CPU THERMD N	11	55
		THERM DIFF	THERMAL	SNS T DP4 DN5	55	
		THERM DIFF	THERMAL	SNS T DN4 DP5	55	
		THERM DIFF	THERMAL	MCP THMDIODE P	21	55
		THERM DIFF	THERMAL	MCP THMDIODE N	21	55
		THERM DIFF	THERMAL	MXM PWRSRC SENSOR P	53	
		THERM DIFF	THERMAL	MXM PWRSRC SENSOR N	53	
		THERM DIFF	THERMAL	SENSE 1V5 S0 P	54	
		THERM DIFF	THERMAL	SENSE 1V5 S0 N	54	
		THERM DIFF	THERMAL	SNS LCD P	55	110
		THERM DIFF	THERMAL	SNS LCD N	55	110
		THERM DIFF	THERMAL	SNS ODD P	55	110
		THERM DIFF	THERMAL	SNS ODD N	55	110
		THERM DIFF	THERMAL	SNS CPU H P	55	
		THERM DIFF	THERMAL	SNS CPU H N	55	
		THERM DIFF	THERMAL	SNS MCP P	55	
		THERM DIFF	THERMAL	SNS MCP N	55	
		THERM DIFF	THERMAL	SNS AMB P	55	110
		THERM DIFF	THERMAL	SNS AMB N	55	110
		THERM DIFF	THERMAL	SNS MXM P	55	
		THERM DIFF	THERMAL	SNS MXM N	55	
		SNS DIFF	THERMAL	VR CPU ISNS1 P	71	72
		SNS DIFF	THERMAL	VR CPU ISNS1 N	71	72
		SNS DIFF	THERMAL	VR CPU ISNS1 R P	71	
		SNS DIFF	THERMAL	VR CPU ISNS1 R N	71	
		SNS DIFF	THERMAL	VR CPU ISNS2 P	71	72
		SNS DIFF	THERMAL	VR CPU ISNS2 N	71	72
		SNS DIFF	THERMAL	VR CPU ISNS2 R P	71	
		SNS DIFF	THERMAL	VR CPU ISNS2 R N	71	
		SNS DIFF	THERMAL	VR CPU ISNS3 P	71	72
		SNS DIFF	THERMAL	VR CPU ISNS3 N	71	72
		SNS DIFF	THERMAL	VR CPU ISNS3 R P	71	
		SNS DIFF	THERMAL	VR CPU ISNS3 R N	71	
1E30			THERMAL	SMC CPU ISENSE	49	53
1E30			THERMAL	VR CPU IOUT	53	71
1E30			THERMAL	VR ISNS CPU P	53	
1E30			THERMAL	VR ISNS CPU N	53	
1E30			THERMAL	SNS PS CPU ISNS	53	
1E30			THERMAL	SMC CPU VSENSE	49	53
1E30			THERMAL	CPU VCC SENSE	12	53
1E30			THERMAL	SMC GPU VSENSE	49	53
1E30			THERMAL	SMC GPU ISENSE	49	53
1E30			THERMAL	SMC 1V5 S0 ISENSE	50	54
1E30			THERMAL	SMC 1V5 S0 ISENSE R	54	
1E30			THERMAL	SMC 1V5 S0 VSENSE	50	54
1E30			THERMAL	SMC MCP CORE ISENSE	50	54
1E30			THERMAL	SMC MCP CORE VSENSE	50	54
1E30			THERMAL	MPCORES0 IMON	54	74
1E30			THERMAL	CPU PECI L	11	55
1E30			THERMAL	SMB PECI L	55	
1E30			THERMAL	CPU PECI MCP	14	55
1E30			THERMAL	HDD OOB TEMP FILT	55	
1E30			THERMAL	HDD OOB TEMP	55	
1E30			THERMAL	HDD OOB TEMP R	55	
1E30			THERMAL	SMC HDD OOB TEMP	55	

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K22/K23 SPECIFIC CONSTRAINTS			
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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA, P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SR	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SR	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_06M_SR	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_06M_SR	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	16L3,16L6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	1SL3,1SL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALL ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2:5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
QND_P2MM	*	0.2 MM	1000
PHR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000













































CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P10M	BGA_P20M
MCP_MEM_COMP	*	BGA_P10M	BGA_P20M
MCP_PEX_COMP	*	BGA_P10M	BGA_P20M

SYNC MASTER=K22		SYNC DATE=09/02/2009	
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K22/K23 RULE DEFINITIONS			
 Apple Inc.		DRAWING NUMBER	D
		051-7863	SIZE
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8	7	6	5	4	3	2	1
FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT							
<div>J4700 USB CAMERA</div> <div>103 47 USB_CAMERA_L_P FUNC_TEST=TRUE</div> <div>103 47 USB_CAMERA_L_N FUNC_TEST=TRUE</div> <div>1 PP5V_S3_REG Testpoint near J4700</div> <div>2 Ground Testpoints near J4700</div>		<div>J5520 ANALOG LCD TEMP SENSOR</div> <div>108 55 SNS_LCD_P FUNC_TEST=TRUE</div> <div>108 55 SNS_LCD_N FUNC_TEST=TRUE</div>		<div>J6601 AUDIO MICROPHONE</div> <div>66 AUD_MIC_IN1_N_CONN FUNC_TEST=TRUE</div> <div>66 GND_AUDIO_MIC1_CONN FUNC_TEST=TRUE</div> <div>66 AUD_MIC_IN1_P_CONN FUNC_TEST=TRUE</div> <div>1 Ground Testpoint near J6601</div>		<div>GND 16 TR16 FUNC_TEST=TRUE</div> <div>RIN_ALLOWED_TPS=1</div>	
<div>J4750 USB CARD READER</div> <div>103 47 USB_SDCARD_L_P FUNC_TEST=TRUE</div> <div>103 47 USB_SDCARD_L_N FUNC_TEST=TRUE</div> <div>1 PP3V3_S3 Testpoint near J4750</div> <div>2 Ground Testpoints near J4750</div>		<div>J5521 AMBIENT TEMP SENSOR</div> <div>108 55 SNS_AMB_P FUNC_TEST=TRUE</div> <div>108 55 SNS_AMB_N FUNC_TEST=TRUE</div>		<div>J6602 AUDIO RIGHT SPEAKER</div> <div>66 AUD_SPKR_OUTLO2R_P FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO2R_N FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO1R_P FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO1R_N FUNC_TEST=TRUE</div>		<div>78 6 PP3V3_S3 2 TR16 FUNC_TEST=TRUE</div> <div>RIN_ALLOWED_TPS=2</div>	
<div>J4720 USB BLUETOOTH</div> <div>103 47 USB_BT_L_P FUNC_TEST=TRUE</div> <div>103 47 USB_BT_L_N FUNC_TEST=TRUE</div> <div>1 PP3V3_S3 Testpoint near J4720</div> <div>2 Ground Testpoints near J4720</div>		<div>J5551 ODD TEMP SENSOR</div> <div>108 55 SNS_ODD_P FUNC_TEST=TRUE</div> <div>108 55 SNS_ODD_N FUNC_TEST=TRUE</div>		<div>J6603 AUDIO LEFT SPEAKER</div> <div>66 AUD_SPKR_OUTLO2L_P FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO2L_N FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO1L_P FUNC_TEST=TRUE</div> <div>66 AUD_SPKR_OUTLO1L_N FUNC_TEST=TRUE</div>		<div>73 6 PP5V_S3_REG 2 TR16 FUNC_TEST=TRUE</div> <div>RIN_ALLOWED_TPS=2</div>	
<div>J4780 IR BOARD</div> <div>103 47 USB_IR_L_P FUNC_TEST=TRUE</div> <div>103 47 USB_IR_L_N FUNC_TEST=TRUE</div> <div>1 PP5V_S3_REG Testpoint near J4780</div> <div>2 Ground Testpoints near J4780</div>		<div>J5600 ODD FAN</div> <div>56 FAN_0_PWR_L FUNC_TEST=TRUE</div> <div>56 FAN_TACH0_L FUNC_TEST=TRUE</div> <div>56 PP12V_S0_FAN0_L FUNC_TEST=TRUE</div> <div>56 FAN_0_GND FUNC_TEST=TRUE</div>					
<div>J4520 SATA ODD (HIGH SPEED)</div> <div>102 45 SATA_ODD_R2D_P FUNC_TEST=TRUE</div> <div>102 45 SATA_ODD_R2D_N FUNC_TEST=TRUE</div> <div>102 45 SATA_ODD_D2R_C_N FUNC_TEST=TRUE</div> <div>102 45 SATA_ODD_D2R_C_P FUNC_TEST=TRUE</div> <div>49 45 SMC_ODD_DETECT FUNC_TEST=TRUE</div> <div>1 PP5V_S0 Testpoint near J4520</div> <div>5 Ground Testpoints near J4520</div>		<div>J5700 CPU FAN</div> <div>57 FAN_2_PWR_L FUNC_TEST=TRUE</div> <div>57 FAN_TACH2_L FUNC_TEST=TRUE</div> <div>57 PP12V_S0_FAN2_L FUNC_TEST=TRUE</div> <div>57 FAN_2_GND FUNC_TEST=TRUE</div>					
<div>J4510 SATA HDD (HIGH SPEED)</div> <div>102 45 SATA_HDD_R2D_P FUNC_TEST=TRUE</div> <div>102 45 SATA_HDD_R2D_N FUNC_TEST=TRUE</div> <div>102 45 SATA_HDD_D2R_C_N FUNC_TEST=TRUE</div> <div>102 45 SATA_HDD_D2R_C_P FUNC_TEST=TRUE</div> <div>3 Ground Testpoints near J4510</div>		<div>J5601 HD FAN</div> <div>56 FAN_1_PWR_L FUNC_TEST=TRUE</div> <div>56 FAN_TACH1_L FUNC_TEST=TRUE</div> <div>56 PP12V_S0_FAN1_L FUNC_TEST=TRUE</div> <div>56 FAN_1_GND FUNC_TEST=TRUE</div>					

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